MONOLITHIC CERAMIC CAPACITORS

CATALOG NO. C-01-D

muRata ERIE®

MURATA ERIE NORTH AMERICA

MURATA ERIE...

is the world's largest manufacturer of ceramic capacitors with an excellent reputation for quality based on years of experience.

U.S. Radial Leaded Monolithic Capacitor Production Facility
Rockmart, Georgia

U.S. Monolithic Capacitor Production Facilities
State College, Pennsylvania

Monolithic Ceramic Capacitor Production Facility
Fukui, Japan

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INTRODUCTION TO SURFACE MOUNT COMPONENTS & TECHNOLOGY

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WHY SURFACE MOUNT COMPONENTS AND TECHNOLOGY?
Surface Mount Technology's growth is being fueled by its inherent advantages:

A) Higher Density – Smaller P.C.B.:
Allows the user to increase the capacity of a given design or decrease the size of the appliance both providing greater function per unit volume.

B) Improved Electrical Performance:
Smaller, leadless components reduce inductance, stray capacitance and increase access speeds.

C) Lower Cost Manufacturing:
Smaller sized components, real estate savings, and elimination of plated-thru-holes in P.C.B.'s can reduce total costs.

D) Automated Assembly:
Leads to greater product consistency, higher reliability and better yields.

E) Physical Standardization:
Components and packaging standards ease product design, allow for automation of process and ensure adequate supply.

F) Higher Resistance to Shock and Vibration:
Due to smaller sized, lighter weight components.

G) Product Synergism:
Achieved where all components of a given product may be available in surface mount configuration compared to past mixtures of leaded and surface mount assembly.

Today, many components and products are being supplied and designed using surface mount technology. However, as with any new, evolving technology, consideration must be given to the too rapid implementation of new techniques.

SOME CONCERNS REGARDING SURFACE MOUNT TECHNOLOGY INCLUDE:

A) Capital Investment:
SMT requires new equipment such as automated and flexible placement machines, perhaps new or revised soldering processes and an array of support conveyors, buffers, and software packages.

B) Testing:
Functional testing of SMT-based boards may be accomplished through edge connectors. However, individual component testing can be difficult due to inaccessibility. Component testing should be considered during product P.C.B. design. In addition, many users are establishing parts per million (ppm) quality programs with component suppliers to greatly reduce or eliminate the need for incoming inspection.

C) Training of Employees:
SMT is a more precise science than conventional thru-board technology and defects are more difficult to observe and repair. Production and Q.C. departments must closely control processes and perform audits to reduce rejects and rework.

D) Materials Compatibility and Availability:
Careful matching of stress related design criteria, particularly for ceramic components is required when implementing SMT. Coefficients of thermal expansion of components and board materials, plus P.C.B. mechanical bending and the effect on components must be considered. Availability of recently designed components may also be a concern.

This section will address the last concern "material compatibility and availability" and provide application guidelines for the use of Murata Erie surface mounted devices.

THE MONOLITHIC CERAMIC CAPACITOR...

Multilayer monolithic ceramic capacitors represent the current state-of-the-art for providing high capacitance per unit volume in a variety of readily available form factors.

Radial devices are compatible with the high speed automatic insertion equipment used in the assembly of printed circuit boards. Unleaded, unencapsulated chip capacitors are also available in tape and reel packaging for high speed automatic placement in hybrid and printed circuit board assemblies.

All monolithic ceramic capacitor form factors begin as a basic chip which consists of alternating layers of ceramic dielectric on which electrodes are printed. The stacked layers are sintered (fired) at very high temperatures to form a single monolithic device. Internal, alternate electrode layers are connected thru common end terminations to form the basic chip capacitor. Leads are attached in radial form to the chip end termination. The bare leaded chip is then encapsulated with an epoxy compound, which meets UL94V-O.

Ceramic dielectric materials of various formulations are available with the most common being COG, X7R and Z5U/Y5V.

COG dielectric formulation is a temperature stable material which exhibits negligible capacitance change with temperature. The material exhibits a low dissipation factor (high Quality factor) and is ideally suited for higher frequency use. Applications include tuned circuitry, timing circuits and medical electronics where long term stability is required.

X7R dielectric formulation is a volumetrically efficient material which exhibits moderate capacitance change over a wide range of temperature, frequency and voltage conditions. Applications include coupling, filtering and bypassing in a variety of electronic circuitry.

Z5U/Y5V dielectric formulation offers the maximum capacitance per unit volume with a capacitance vs temperature characteristic that varies widely. Most common applications are for coupling and bypass use.

Murata Erie North America's State College facility represents the state-of-the-art in volume manufacture of leaded and chip multi-layer ceramic capacitors. Features of all Murata Erie multi-layer ceramic capacitor facilities include:

- highly automated manufacturing process.
- class 10,000 or better clean room front end operations
- 100% electrical testing for all components
- continuous QC inspection and audits of all materials and processes
- complete test facilities (DPA, various scanning techniques, etc.)

Our manufacturing facilities lend themselves ideally to the production of the highest quality multi-layer ceramic capacitors in the world. This factor has led to our acceptance as a "parts per million" (ppm) supplier by a number of our valued customers.

Murata Erie's comprehensive line of monolithic ceramic capacitors represented in this catalog can meet virtually every application requirement. In addition to the standard COG, X7R and Z5U/Y5V dielectric formulations, a wide range of temperature compensating and high "K" dielectric units are also available.

If a device to meet a specific requirement is not illustrated in this catalog, contact Murata Erie's nearest sales office. Our application and customer engineering personnel stand ready to help!

GLOSSARY OF SPECIALIZED CAPACITOR TERMS

1–DIELECTRIC:
Sometimes called "Insulator," a dielectric is a material whose internal charges are bound and can therefore only move over atomic dimensions. It separates the conductive capacitor plates and is important in determining temperature characteristics, voltage rating, capacity/volume and other characteristics of a capacitor.

2–DISSIPATION FACTOR ("DF"):
The dissipation factor of an insulating material is defined as the ratio of energy dissipated to energy stored in the dielectric. The DF is frequency sensitive and must be specified at a given frequency.

3–QUALITY FACTOR ("Q"):
The Q factor is the ratio of energy stored to energy dissipated and is therefore often taken as the inverse of the DF at low frequency. Sometimes called "Figure of Merit," Q factors must be specified at a given frequency.

4–WORKING (OR "RATED") VOLTAGE:
Nominal continuous voltage which may be applied to a component with no derating of any kind.

5–DIELECTRIC WITHSTANDING VOLTAGE:
The peak voltage which the component is designed to withstand without damage for short periods of time. This value must be specified in terms of frequency, waveform, and time.

6–INSULATION RESISTANCE (IR):
I.R. is the terminal to terminal DC resistance of a capacitor, and must be specified in terms of voltage, temperature, and relative humidity.

Typically expressed as a minimum resistance or as an R•C product.

Example of IR expressed using R•C product: If a material is rated at 500 Ω•F, also expressed as 500MΩ•μF

For 1.0 μF	IR ≥	500 MΩ
0.1 μF	≥	5000 MΩ
0.01 μF	≥	50,000 MΩ

7–TEMPERATURE COEFFICIENT ("TC"):
"TC" is the decimal change in capacity per degree change in environmental temperature. Some dielectrics are very lossy and generate internal heat and for that reason this test is conventionally conducted under "no load" conditions. The standard definition for "TC" in parts per million per degree centigrade is...

$$TC = \frac{(Cx - Co)}{Co} \times \frac{(10^6)}{(Tx - To)} /^{\circ}C$$

Where "Tx" is the test temperature, "To" is the reference temperature—usually 25°C. "Co" is the capacity measured at the reference temperature and "Cx" is the capacity measured at the test temperature.

8–DRIFT:
The extent in pF or % to which capacitor changes value as a result of temperature exposure. Sometimes called "Retrace," this measurement is usually made under nominal (i.e. room) conditions and is accomplished both before and after the conclusion of temperature excursion. (Note: "Drift" may occasionally be used in the test context of the simple passage of time).

9–TOLERANCE OF CAPACITANCE:
Is defined as the maximum percentage of deviation from the nominal capacitance value when measured at a standard temperature, voltage and frequency.

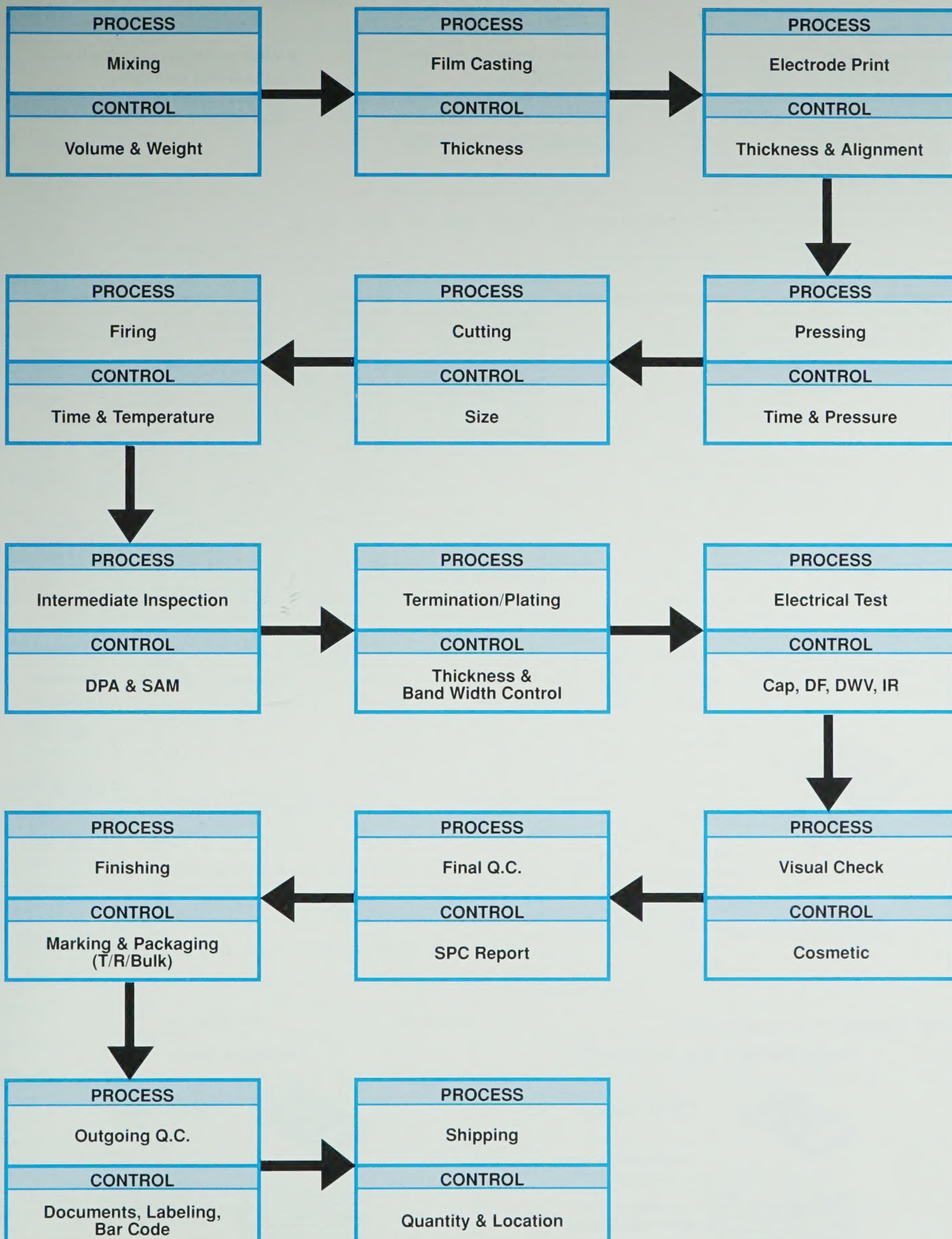
10–TERMINATION:
This term refers to the material and/or geometry of the terminals of the capacitor.

11–CHIP, MONOLITHIC OR MULTI-LAYER CAPACITOR (MLC):
All of these terms, and any combination of them, refer to a ceramic capacitor style which consists of alternate layers of ceramics and conductive (metallic) surfaces which are compressed and vitrified to form a single "monolithic" structure. Alternate metallic surfaces are then interconnected to form a two terminal capacitor.

12–ESR:
The sum of the equivalent series resistances of the electrode resistance and loss tangent of the dielectric, otherwise known as the real part of the capacitors equivalent circuit impedence (Note: The dielectric loss tangent is frequency dependent as is ESR).

13–AGING:
Aging is the change in the dielectric constant as a function of time. Aging is particularly noticeable in high dielectric materials and is measured as a percentage change per decade of time. Aging decreases logarithmically and becomes less apparent with time.

MANUFACTURING FLOW DIAGRAM



COG AND TEMPERATURE COMPENSATING

FEATURES

- Miniature size
- No Polarity
- Nickel Barrier Termination Standard – highly resistant to metal migration
- Uniform dimensions and configuration
- Flow and Reflow Solderable
- Minimum series inductance
- Tape and Reel Packaging
- Wide selection of capacitance values and voltages
- Largest production capacity and volumn in the world

PART NUMBERING SYSTEM

GRM 40 --- COG 101 K 050 A D

CAPACITOR TYPE AND SIZE
See below and following pages.

3-digit code appears as necessary to indicate special thickness requirements. Please consult your local sales office for details.

TEMPERATURE CHARACTERISTICS
COG
P2H
R2H
S2H
T2H
U2J
SL

CAPACITANCE VALUE
Expressed in picofarads and identified by a three-digit number. First two digits represent significant figures. Last digit specifies the number of zeros to follow. For fractional values below 10pF, the letter "R" is used as the decimal point and the last digit becomes significant.

CAPACITANCE TOLERANCE
(10pF or less)
B=±.1pF
C=±.25pF
D=±.5pF
F=±1pF for 10pF only
(over 10pF)
F=±1%
G=±2%
J=±5%
K=±10%

VOLTAGE
Identified by a three-digit number.

MARKING
A=Unmarked
B=EIA Marking
C=Non-standard
Contact Factory.

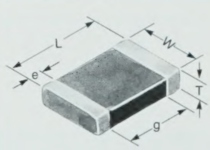
PACKAGING

Reel Diameter/ Tape Material	Code
7" Paper Tape	D
7" Plastic Tape	L
13" Paper Tape	J
13" Plastic Tape	K
Bulk	B

See pages 24-25 for additional marking and packaging information
T/R per EIA-481-1

CHIP DIMENSIONS

DIMENSIONS: in (mm)



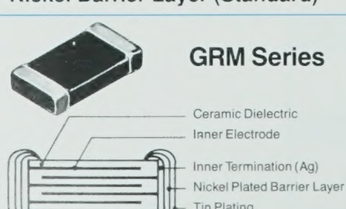
Size	EIA Code	L Length	W Width	T Thickness	g (Min.) Insulation	e Termination
GRM39	0603	.060 ± .066 (1.6 ± 0.15)	.030 ± .006 (0.80 ± 0.15)	Note 1: Thickness varies with capacitance value. See capacitance charts on following pages for thickness.	.020 (0.5)	.014±..006 (0.35±0.15)
GRM40	0805	.080±.006 (2.0±0.15)	.050±.006 (1.25±0.15)		.030 (0.75)	.020±.010 (0.5±0.25)
GRM42-6	1206	.125±.006 (3.2±0.15)	.063±.006 (1.6±0.15)		.040 (1.0)	020±.010 (0.5±0.25)
GRM42-2	1210	.125±.006 (3.2±0.15)	.100±.006 (2.5±0.15)		.040 (1.0)	.020±.010 (0.5±0.25)
GRM43-2	1812	.180±.012 (4.6±0.3)	.125±.008 (3.2±0.2)		.080 (2.0)	.025±.015 (0.63±0.38)
GRM43-4	1825	.180±.012 (4.6±0.3)	.250±.016 (6.35±0.4)		.080 (2.0)	.025±0.15 (0.63±0.38)
GRM44-1	2220*	.220±.012 (5.6±0.3)	.200+.010-.025 (5.1+0.25-0.5)		.080 (2.0)	.025±.015 (0.63±0.38)
GRM44	2225*	.220±.012 (5.6±0.3)	.250±.016 (6.35±0.4)		.080 (2.0)	.025±.015 (0.63±0.38)

*Non EIA–Standard Size

CHIP TERMINATION DIAGRAMS

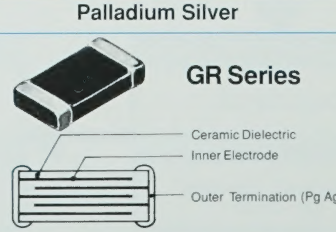
Nickel Barrier Layer (Standard)

GRM Series



Palladium Silver

GR Series



Note: Other Terminations Available Upon Request. Please Contact Local Sales Office.

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COG AND TEMPERATURE COMPENSATING

GENERAL

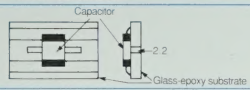
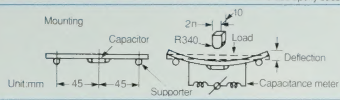
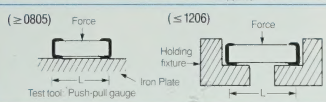
Temperature Coefficient	Temperature Range
COG = 0 ± 30 ppm*	−55° to +125°C
P2H = N150 ± 60 ppm	−55° to +85°C
R2H = N220 ± 60 ppm	−55° to +85°C
S2H = N330 ± 60 ppm	−55° to +85°C
T2H = N470 ± 60 ppm	−55° to +85°C
U2J = N750 ± 120 ppm	−55° to +85°C
SL = N1000 to P350	−55° to +85°C

***TC Tolerance for COG**
0.5 to 2.0pf = ±250ppm(K)
2.1 to 3.9pf = ±120ppm(J)
4.0 to 9.9pf = ± 60ppm(H)
10 or over = ± 30ppm(G)
Refer to EIA-RS198 for other limitations

ELECTRICAL

TEST	
Capacitance & Q (Frequency & Voltage):	≤1000pF 1 KHz ± 100Hz @ 1.0 ± .2 Vrms >1000pF 1MHz ± 100 KHz @ 1.0 ± .2 Vrms
Q Limits	≤30pF: 400 + (20xC (pF)) >30pF: 1000 minimum
Insulation Resistance (I.R.)	100,000 megohms or 1000 megohms – mfd (whichever is less) with rated voltage applied for 2 minutes max with 50mA limiting current
Dielectric Strength (Flash)	250% of rated voltage for 5 seconds with series resistor limiting charging current to 50mA max.
Aging	Negligible

MECHANICAL

<table>
<tr><th>TEST</th><th>TEST METHOD</th><th colspan="6">POST TEST LIMITS</th></tr>
<tr><td>Terminal Adhesion</td><td></td><td colspan="6"><0603 1.0 lbs.
≥0805 2.2 lbs.
No evidence of termination peeling</td></tr>
<tr><td>Deflection</td><td></td><td colspan="6">2 mm deflection (paper phenol board)
1mm deflection (Glass epoxy board)
No mechanical damage
Cap., DF, IR meet initial limits</td></tr>
<tr><td rowspan="2">Break Strength</td><td rowspan="2">Stress is applied at rate of 150mm/minute</td><td colspan="3">Thickness (mm)</td><td colspan="3">F. minimum (lbs)</td></tr>
<tr><td colspan="3">0.7, 0.8
1.0
≤ 1.25</td><td colspan="3">1.8
6.6
12.0</td></tr>
<tr><td rowspan="4">Solderability</td><td rowspan="4">MIL-STD-202
Method 208F</td><td colspan="6">Solder coverage GRM Type</td></tr>
<tr><td></td><td colspan="2">Under Room temperature</td><td>Under high temperature</td><td colspan="2">Under high humidity</td></tr>
<tr><td>Initial</td><td>6 months</td><td>12 months</td><td>85°C 100 hrs</td><td colspan="2">40°C, 90-95%RH 100hrs.</td></tr>
<tr><td>95-100%</td><td>95-100%</td><td>95%</td><td>90-95%</td><td colspan="2">95%</td></tr>
</table>

ENVIRONMENTAL

<table>
<tr><th>TEST</th><th colspan="2">TEST METHOD</th><th>POST TEST LIMITS</th></tr>
<tr><td>Thermal Shock (Air to Air)</td><td colspan="2">MIL-STD-202, Method 107, Condition A
Prior to starting Thermal Shock test, capacitors shall be heat treated (deaged) for one (1) hour at 150°C. Allow capacitors to stabilize at room temperature for 24 hours prior to taking initial measurements.

Post thermal Shock measurement shall be taken after 24 hours stabilization.</td><td>Appearance: No visual damage

ΔC: = ±2.0% or ±0.5pF (whichever is greater)
Q: >30pF=1,000 min., ≤ 30pF = 400 + [20 × C(pF)]
I.R.: = 100,000MΩ min. or 1,000MΩ•μF (whichever is less)</td></tr>
<tr><td rowspan="2">Humidity</td><td>RATED VOLTAGE</td><td>LOW VOLTAGE</td><td rowspan="2">Appearance: No defects
Capacitance: ±3% or ±.3pF (whichever is less)
Q :>30pF = 500 min., ≤30pF = 200 + [10 x C(pF)]
I.R.: 10,000 megohms or 100 megohm-mfd. (whichever is less)
Flash: 250% rated voltage</td></tr>
<tr><td>Apply rated voltage for 500 ±12 hours at 85°C and 85% relative humidity

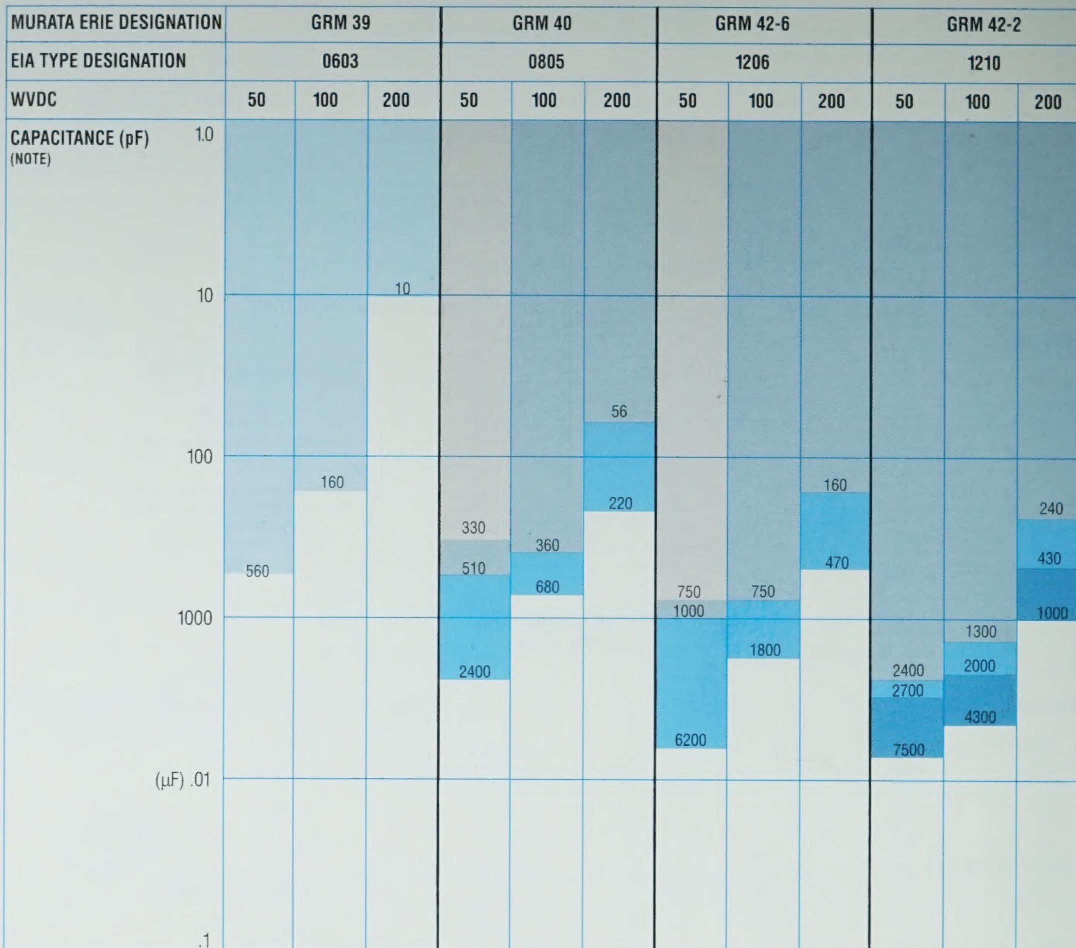
See Note 1</td><td>Apply .5 Vrms for 250 ±12 hours at 85°C and 85% relative humidity

See Note 1</td></tr>
<tr><td>Life Test</td><td colspan="2">Apply 200% of rated voltage for 1000 ± 12 hours at maximum operating temperature

See Note 2</td><td>Appearance: No defects
Capacitance: ±3% or ±.3pF (whichever is greater)
Q : >30pF = 500 min., ≤30pF = 200 + [10 x C(pF)]
I.R.: 10,000 megohms or 100 megohm-mfd. (whichever is less)
Flash: 250% rated voltage</td></tr>
</table>

Note 1: Upon completion of either above test wait 24 hours prior to performing post testing.
Note 2: Upon completion of above test wait 24 hours prior to performing post testing.

COG



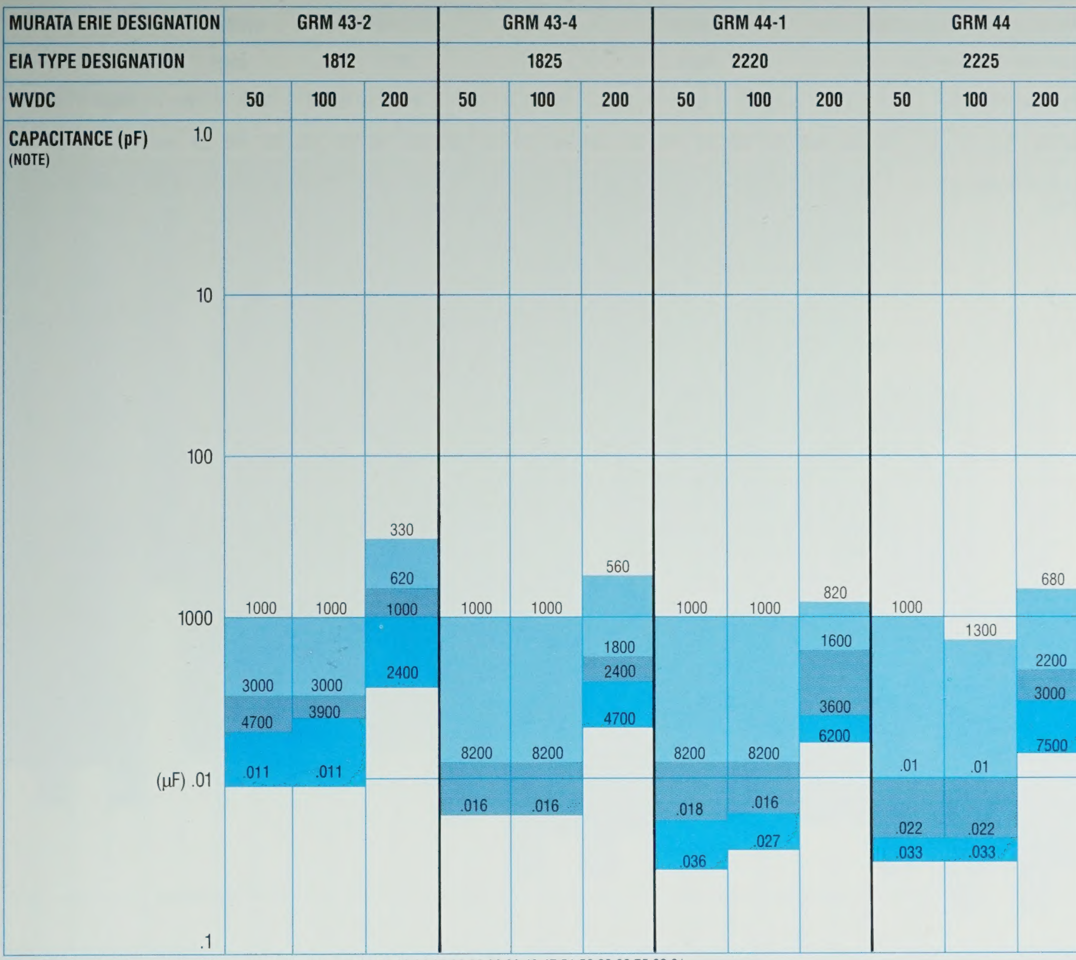
Note: Capacitance values = EIA 24 Step = 10,11,12,13,15,16,18,20,22,24,27,30,33,36,39,43,47,51,56,62,68,75,82,91
For values under 1.0pF and other values not listed, contact your local Murata Erie Sales Office

STANDARD THICKNESS/PACKAGING SPECIFICATIONS

Dimensions (mm)	Bulk	Tape			
	Pcs/bag (typical)	Pcs/7 inch (178 mm) reel		Pcs/13 inch (330 mm) reel	
	Plastic	Paper	Embossed	Paper	Embossed
$T: 0.7^{+0}_{-0.2}$	1000	4000	4000	10000	10000
$T: 0.8 \pm 0.1$	1000	4000	N/A	10000	N/A
$T: 1.0^{+0}_{-0.2}$	1000	4000	3000	10000	10000
$T: 1.25^{+0}_{-0.2}$*	1000	N/A	3000	N/A	10000
$T: 1.5^{+0}_{-0.2}$	1000	N/A	2000	N/A	8000

*GRM 40 T = 1.25 ± .1

COG



Note: Capacitance values = EIA 24 Step = 10,11,12,13,15,16,18,20,22,24,27,30,33,36,39,43,47,51,56,62,68,75,82,91
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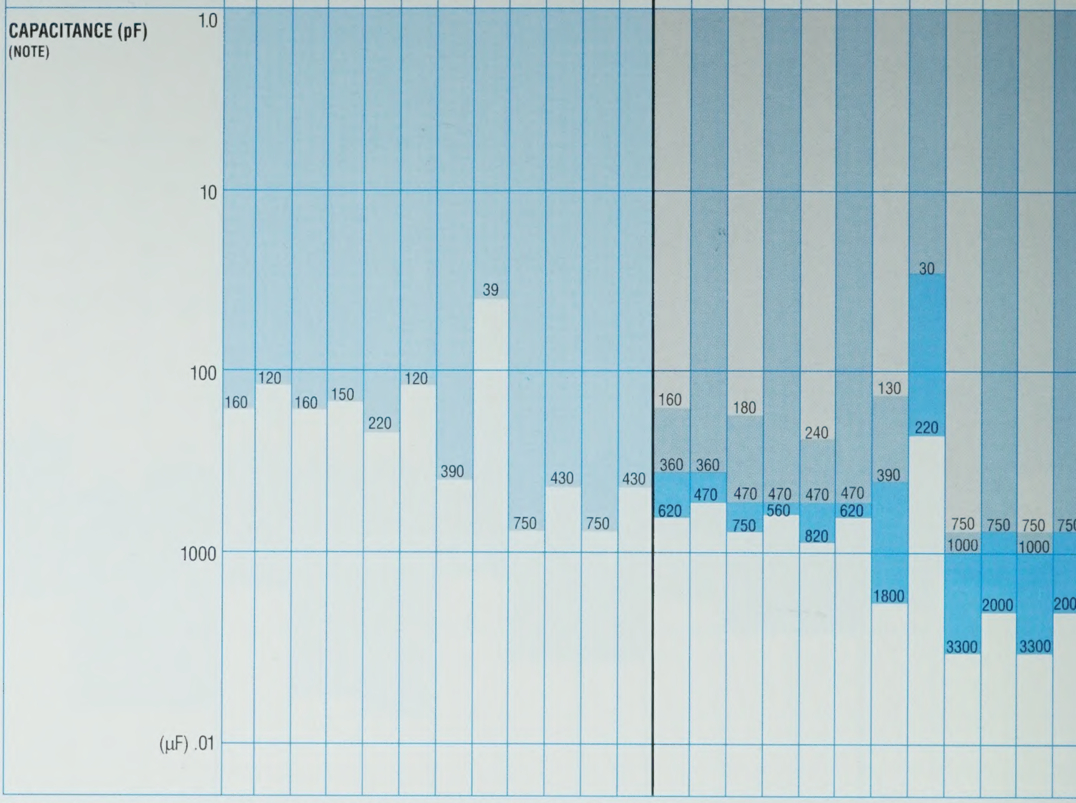
STANDARD THICKNESS/PACKAGING SPECIFICATIONS

Dimensions (mm)	Bulk	Tape			
	Pcs/bag (typical)	Pcs/7 inch (178 mm) reel		Pcs/13 inch (330 mm) reel	
	Plastic	Paper	Embossed	Paper	Embossed
T : 1.25 $^{+0}_{-0.2}$	1000	N/A	1000	N/A	5000
T : 1.5 $^{+0}_{-0.2}$	1000	N/A	1000	N/A	5000
T : 2.0 $^{+0}_{-0.2}$	1000	N/A	1000	N/A	4000

TEMPERATURE COMPENSATING

MURATA ERIE DESIGNATION	GRM 39												GRM 40											
EIA TYPE DESIGNATION	0603												0805											
CHARACTERISTIC	P2H		R2H		S2H		T2H		U2H		SL		P2H		R2H		S2H		T2H		U2J		SL	
WVDC	50	100	50	100	50	100	50	100	50	100	50	100	50	100	50	100	50	100	50	100	50	100	50	100



Note: Capacitance values = EIA 24 Step = 10,11,12,13,15,16,18,20,22,24,27,30,33,36,39,43,47,51,56,62,68,75,82,91
For values under 1.0pF and other values not listed, contact your local Murata Erie Sales Office

STANDARD THICKNESS/PACKAGING SPECIFICATIONS

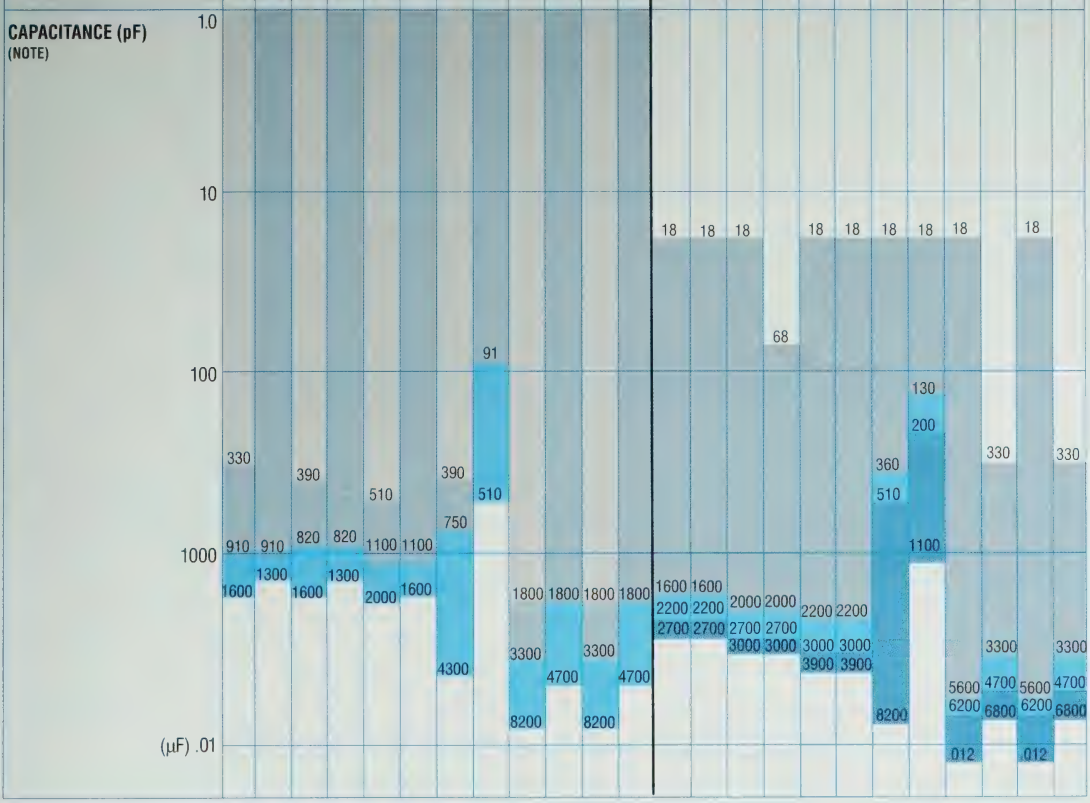
Dimensions (mm)	Bulk	Tape			
	Pcs/bag (typical)	Pcs/7 inch (178 mm) reel		Pcs/13 inch (330 mm) reel	
	Plastic	Paper	Embossed	Paper	Embossed
T : 0.7 $^{+0}_{-0.2}$	1000	4000	4000	10000	10000
T : 0.8 ±0.1	1000	4000	N/A	10000	N/A
T : 1.0 $^{+0}_{-0.2}$	1000	4000	3000	10000	10000
T : 1.25 $^{+0}_{-0.2}$*	1000	N/A	3000	N/A	10000
T : 1.5 $^{+0}_{-0.2}$	1000	N/A	2000	N/A	8000

*GRM 40 T = 1.25 ± .1

TEMPERATURE COMPENSATING

MURATA ERIE DESIGNATION	GRM 42-6												GRM 42-2											
EIA TYPE DESIGNATION	1206												1210											
CHARACTERISTIC	P2H		R2H		S2H		T2H		U2J		SL		P2H		R2H		S2H		T2H		U2J		SL	
WVDC	50	100	50	100	50	100	50	100	50	100	50	100	50	100	50	100	50	100	50	100	50	100	50	100

CAPACITANCE (pF)
(NOTE)



Note: Capacitance values = EIA 24 Step = 10,11,12,13,15,16,18,20,22,24,27,30,33,36,39,43,47,51,56,62,68,75,82,91
For values under 1.0pF and other values not listed, contact your local Murata Erie Sales Office

STANDARD THICKNESS/PACKAGING SPECIFICATIONS

Dimensions (mm)	Bulk	Tape			
	Pcs/bag (typical)	Pcs/7 inch (178 mm) reel		Pcs/13 inch (330 mm) reel	
	Plastic	Paper	Embossed	Paper	Embossed
T : 0.7 $^{+0}_{-0.2}$	1000	4000	4000	10000	10000
T : 0.8 ±0.1	1000	4000	4000	10000	10000
T : 1.0 $^{+0}_{-0.2}$	1000	4000	3000	10000	10000
T : 1.25 $^{+0}_{-0.2}$	1000	N/A	3000	N/A	10000
T : 1.5 $^{+0}_{-0.2}$	1000	N/A	2000	N/A	8000

CHIPS–
GRM Series

HIGH DIELECTRIC CONSTANT TYPE

PART NUMBERING SYSTEM

GRM 40 --- X7R 103 K 050 A D

CAPACITOR TYPE AND SIZE
See below and following pages.

--- 3-digit code appears as necessary to indicate special thickness requirements. Please consult your local sales office for details.

TEMPERATURE CHARACTERISTICS
X7R
Z5U
Y5V

CAPACITANCE VALUE
Expressed in picofarads and identified by a three-digit number. First two digits represent significant figures. Last digit specifies the number of zeros to follow.

CAPACITANCE TOLERANCE
X7R: J=±5% on special request
K=±10%
M=±20%
Z5U: M=±20%
Z+80, -20%
Y5V: Z+80, -20%

VOLTAGE
Identified by a three-digit number.

MARKING
A=Unmarked
B=EIA Marking
C=Non-standard Contact Factory.

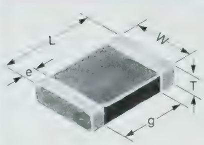
PACKAGING

Reel Diameter/ Tape Material	Code
7" Paper Tape	D
7" Plastic Tape	L
13" Paper Tape	J
13" Plastic Tape	K
Bulk	B

See pages 24-25 for additional marking and packaging information
T/R per EIA-481-1

CHIP DIMENSIONS

DIMENSIONS: in (mm)



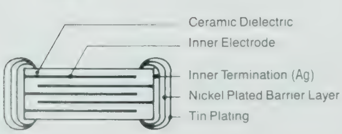
Size	EIA Code	L Length	W Width	T Thickness	g (Min.) Insulation	e Termination
GRM39	0603	.060 ± .066 (1.6 ± 0.15)	.030 ± .006 (0.80 ± 0.15)	Note 1: Thickness varies with capacitance value. See capacitance charts on following pages for thickness.	.020 (0.5)	.014±..006 (0.35±0.15)
GRM40	0805	.080 ± .006 (2.0 ± 0.15)	.050 ± .006 (1.25 ± 0.15)		.030 (0.75)	.020±.010 (0.5±0.25)
GRM42-6	1206	.125 ± .006 (3.2 ± 0.15)	.063 ± .006 (1.6 ± 0.15)		.040 (1.0)	.020±.010 (0.5±0.25)
GRM42-2	1210	.125 ± .006 (3.2 ± 0.15)	.100 ± .006 (2.5 ± 0.15)		.040 (1.0)	.020±.010 (0.5±0.25)
GRM43-2	1812	.180 ± .012 (4.6 ± 0.3)	.125 ± .008 (3.2 ± 0.2)		.080 (2.0)	.025±.015 (0.63±0.38)
GRM43-4	1825	.180±.012 (4.6±0.3)	.250±.016 (6.35±0.4)		.080 (2.0)	.025±0.15 (0.63±0.38)
GRM44-1	2220*	.220 ± .012 (5.6 ± 0.3)	.200+.010-.025 (5.1+0.25-0.5)		.080 (2.0)	.025±.015 (0.63±0.38)
GRM44	2225*	.220 ± .012 (5.6 ± 0.3)	.250 ± .016 (6.35 ± 0.4)		.080 (2.0)	.025±.015 (0.63±0.38)

*Non EIA–Standard Size

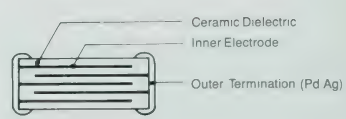
CHIP TERMINATION DIAGRAMS

Nickel Barrier Layer (Standard)	Palladium Silver
GRM Series	GR Series

GRM Series



GR Series



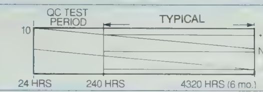
Note: Other Terminations Available Upon Request. Please Contact Local Sales Office.

muRata ERIE

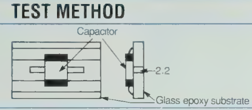
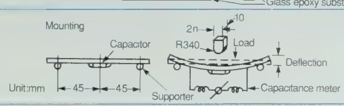
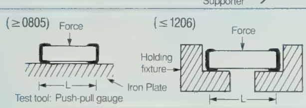
HIGH DIELECTRIC CONSTANT TYPE

GENERAL/ELECTRICAL

Capacitance Change with Temperature:	X7R: ±15% ΔCX -55°C to +125°C Z5U: $^{+22\%}_{-56\%}$ ΔCX + 10°C to +85°C Y5V: $^{+22\%}_{-82\%}$ ΔCX - 30°C to +85°C
Capacitance & D.F. (Frequency & Voltage)	X7R: 1KHz ±100Hz @ 1.0 ±.2 Vrms Z5U: } 1KHz ±100Hz @ .5 ±.1 Vrms Y5V: }
Dissipation Factor (D.F.)	25 to 100V / 16V X7R 2.5% 3.5% Z5U 3.0% – Y5V 5.0% 7.0%

Insulation Resistance (I.R.)	X7R 100,000 megohms or 1000 megohm-mfd (whichever is less) Z5U/Y5V 10,000 megohms or 500 megohm-mfd (whichever is less)
Dielectric Strength (Flash)	250% of rated voltage for 5 seconds with series resistor limiting charge current to 50mA Max
Aging (per Decade) **X7R 3%** **Z5U 5%** **Y5V 7%**	

MECHANICAL

TEST	TEST METHOD	POST TEST LIMITS
Terminal Adhesion		<0603 1.0 lbs. ≥0805 2.2 lbs. No evidence of termination peeling
Deflection		2 mm deflection (paper phenol board) 1mm deflection (Glass epoxy board) No mechanical damage Cap., DF, IR meet initial limits
Break Strength	 Stress is applied at rate of 150mm/minute	Thickness (mm) / Minimum (lbs) 0.7, 0.8 / 1.8 1.0 / 4.4 ≤1.25 / 12.0
Solderability	MIL-STD-202 Method 208F	see Solder coverage GRM Type table

Solder coverage GRM Type

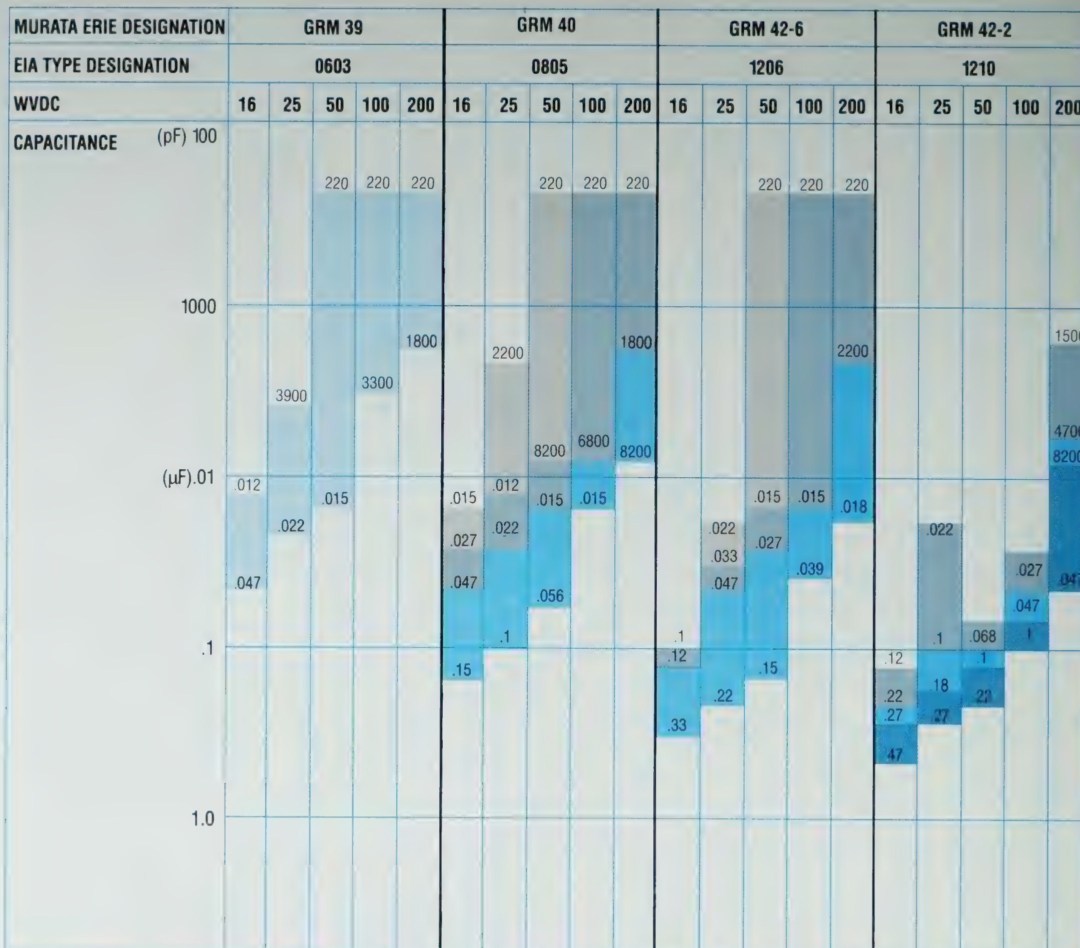
	Under Room temperature		Under high temperature	Under high humidity
Initial	6 months	12 months	85°C 100 hrs	40°C, 90-95%RH 100hrs
95-100%	95-100%	95%	90-95%	95%

ENVIRONMENTAL

TEST	TEST METHOD		POST TEST LIMITS
Thermal Shock (Air to Air)	MIL-STD-202, Method 107, Condition A Prior to starting Thermal Shock test, capacitors shall be heat treated (deaged) for one (1) hour at 150°C. Allow capacitors to stabilize at room temperature for 24 hours prior to taking initial measurements. Post thermal Shock measurement shall be taken after 24 hours stabilization.		Appearance: No visual damage Δ C: X7R=±12.5% Z5U=±20.0% Y5V=±30.0% D.F.: X7R=2.5% max. @ 25°C, (3.5% max. @ 25 C for GR,16V Series) Z5U=3.0% max. @ 25°C, Y5V=5.0% max. @ 25°C, (7.0% max. @ 25°C for GR,16V Series) I.R.: X7R=100,000MΩ min. or 1,000MΩ•μF (whichever is less) Z5U/Y5V=10,000Ω or 500MΩ•μF min. (whichever is less)
	RATED VOLTAGE	**LOW VOLTAGE**	
Humidity	Apply rated voltage for 500 ±12 hours at 85°C and 85% relative humidity **See Note 1**	Apply .5 Vrms for 250 ±12 hours at 85°C and 85% relative humidity **See Note 1**	Appearance: No defects Capacitance: X7R ± 12% Δ CX, Z5U/Y5V ± 30% Δ CX DF: X7R = 3.0% max. @ 25°C, (5% max. at 25°C for 16V Series) Z5U = 3.5% max. @ 25°C Y5V = 7.5% max. @ 25°C, (10% max. at 25°C for 16V Series) I.R.: X7R 10,000MΩ or 100MΩ-mfd. (whichever is less) Z5U/Y5V 1,000MΩ or 50MΩ-mfd. (whichever is less) Flash: 250% rated voltage
Life Test	Apply 200% of rated voltage for 1000 ± 12 hours at maximum operating temperature **See Note 2**		Appearance: No defects Capacitance: X7R ± 12% Δ CX, Z5U/Y5V ± 30% Δ CX DF: X7R = 3.0% max. @ 25°C, (5% max. at 25°C for 16V Series) Z5U = 3.5% max. @ 25°C Y5V = 7.5% max. @ 25°C, (10% max. at 25°C for 16V Series) I.R.: X7R 1,000MΩ or 50MΩ-mfd. (whichever is less) Z5U/Y5V 1,000MΩ or 50MΩ-mfd. (whichever is less) Flash: 250% rated voltage

Note 1: Upon completion of either above test wait 24 hours prior to performing post testing.
Note 2: Upon completion of above test wait 24 hours prior to performing post testing.

HIGH DIELECTRIC CONSTANT TYPE X7R



Note: Capacitance values = EIA 12 Step = 10, 12, 15,18, 22, 27, 33, 39, 47, 56, 68, 82. For values not listed, contact your local Murata Erie Sales Office.

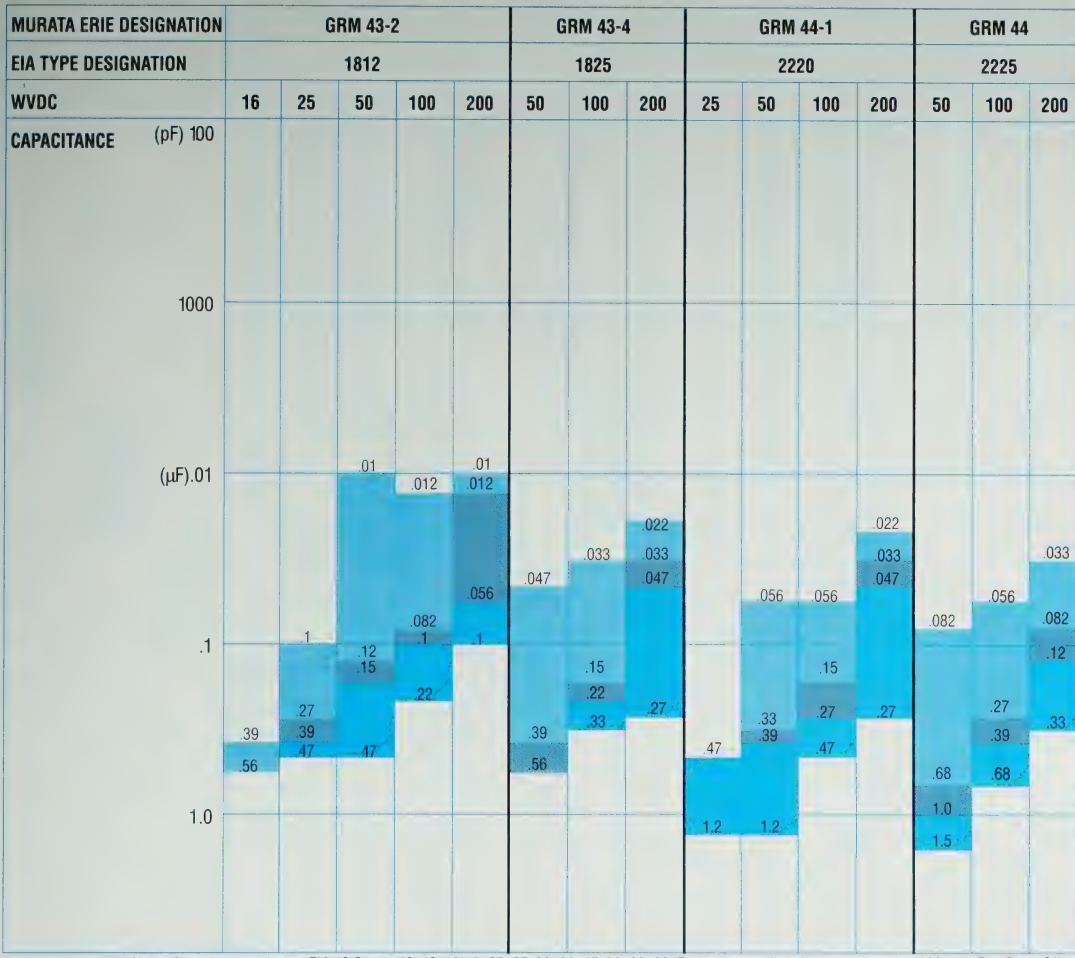
STANDARD THICKNESS/PACKAGING SPECIFICATIONS

DIMENSIONS: mm	Bulk	Tape			
	Pcs/bag (typical)	Pcs/7 inch (178 mm) reel		Pcs/13 inch (330 mm) reel	
	Plastic	Paper	Embossed	Paper	Embossed
$T: 0.7^{+0}_{-0.2}$	1000	4000	4000	10000	10000
$T: 0.8 \pm 0.1$	1000	4000	N/A	10000	N/A
$T: 1.0^{+0}_{-0.2}$	1000	4000	3000	10000	10000
$T: 1.25^{+0}_{-0.2}$*	1000	N/A	3000	N/A	10000
$T: 1.5^{+0}_{-0.2}$	1000	N/A	2000	N/A	8000

*GRM 40 T = 1.25 ± .1

muRata ERiE

HIGH DIELECTRIC CONSTANT TYPE X7R



Note: Capacitance values = EIA 12 Step = 10, 12, 15,18, 22, 27, 33, 39, 47, 56, 68, 82. For values not listed, contact your local Murata Erie Sales Office.

STANDARD THICKNESS/PACKAGING SPECIFICATIONS

DIMENSIONS: mm	Bulk	Tape			
	Pcs/bag (typical)	Pcs/7 inch (178 mm) reel		Pcs/13 inch (330 mm) reel	
	Plastic	Paper	Embossed	Paper	Embossed
T : 1.25 $^{+0}_{-0.2}$	1000	N/A	1000	N/A	5000
T : 1.5 $^{+0}_{-0.2}$	1000	N/A	1000	N/A	5000
T : 2.0 $^{+0}_{-0.2}$	1000	N/A	1000	N/A	4000

CHIPS–
GRM Series

HIGH DIELECTRIC CONSTANT TYPE Z5U

Note: Capacitance values = EIA 6 Step = 10, 15, 22, 33, 47, 68. For values not listed, contact your local Murata Erie Sales Office.

STANDARD THICKNESS/PACKAGING SPECIFICATIONS

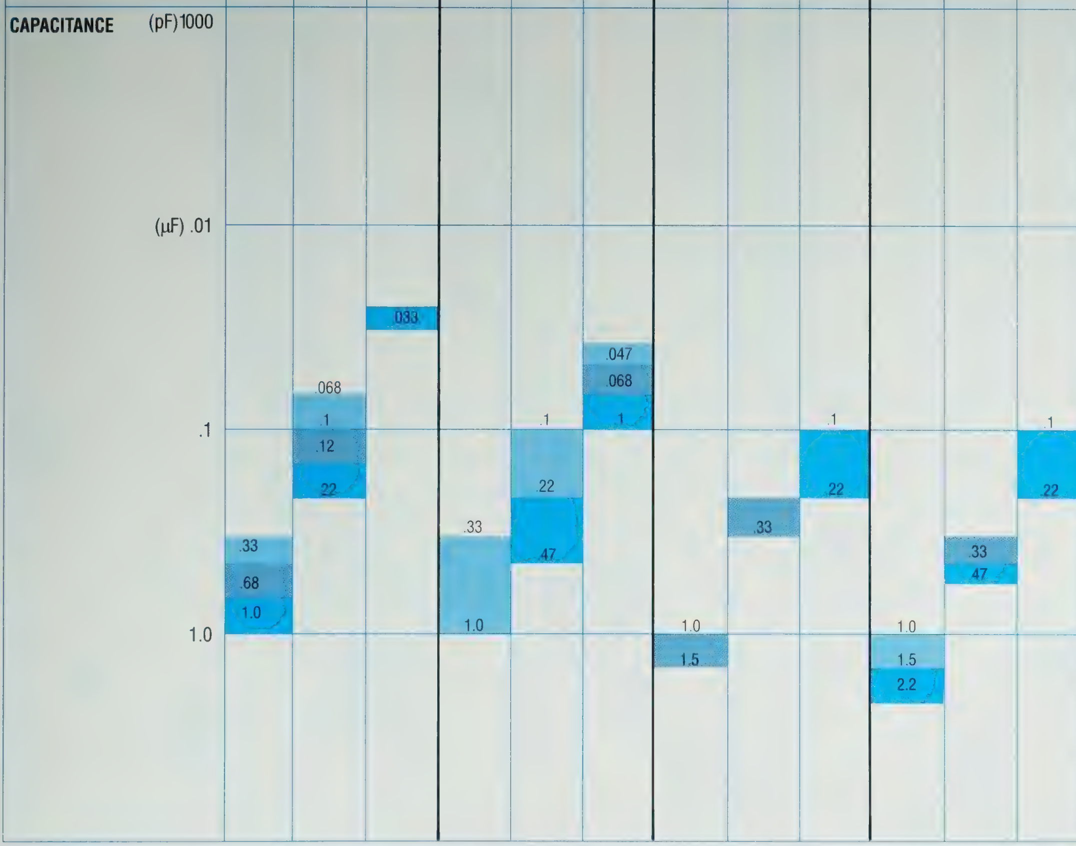
DIMENSIONS: mm	Bulk	Tape			
	Pcs/bag (typical)	Pcs/7 inch (178 mm) reel		Pcs/13 inch (330 mm) reel	
	Plastic	Paper	Embossed	Paper	Embossed
T : 0.7 $^{+0}_{-0.2}$	1000	4000	4000	10000	10000
T : 0.8 ±0.1	1000	4000	N/A	10000	N/A
T : 1.0 $^{+0}_{-0.2}$	1000	4000	3000	10000	10000
T : 1.25 $^{+0}_{-0.2}$*	1000	N/A	3000	N/A	10000
T : 1.5 $^{+0}_{-0.2}$	1000	N/A	2000	N/A	8000

*GRM40 T= 1.25 ± .1

muRata ERiE

HIGH DIELECTRIC CONSTANT TYPE Z5U

MURATA ERIE DESIGNATION	GRM 43-2			GRM 43-4			GRM 44-1			GRM 44		
EIA TYPE DESIGNATION	1812			1825			2220			2225		
WVDC	50	100	200	50	100	200	50	100	200	50	100	200

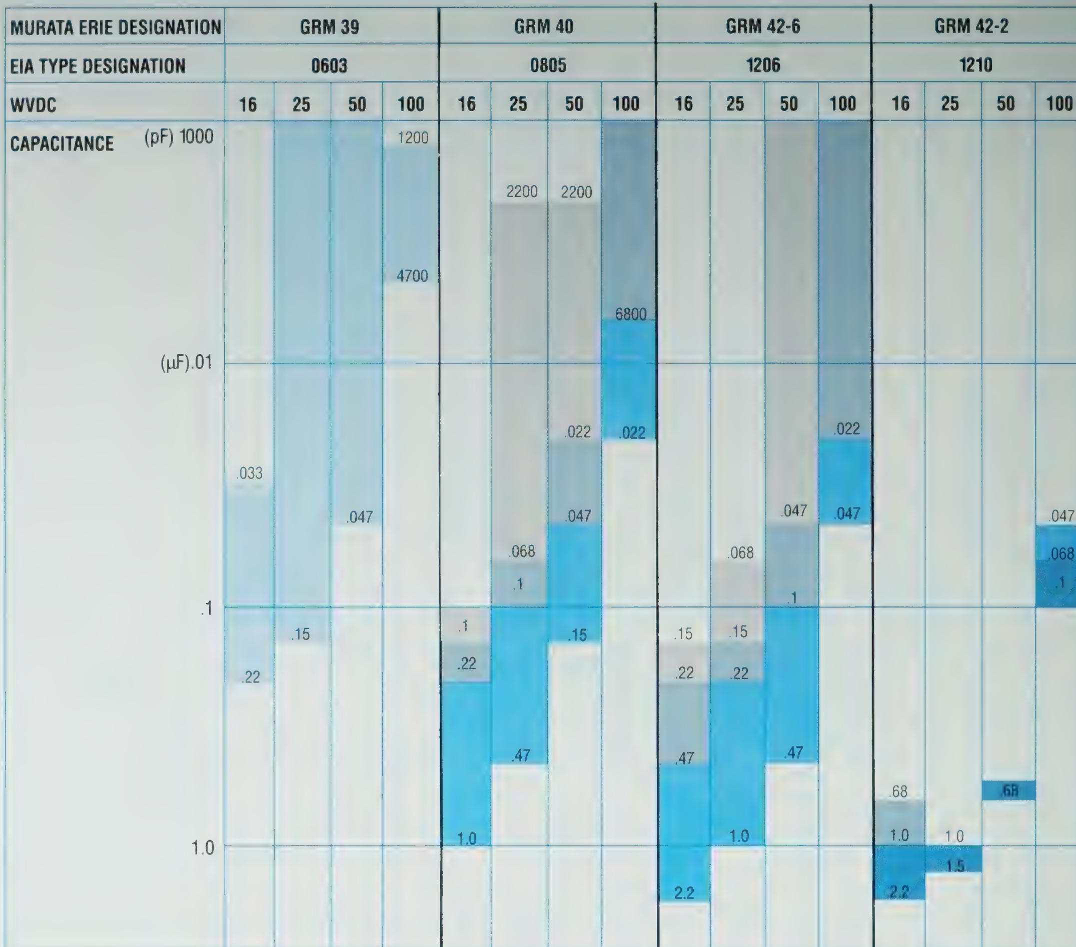


Note: Capacitance values = EIA 6 Step = 10, 15, 22, 33, 47, 68. For values not listed, contact your local Murata Erie Sales Office.

STANDARD THICKNESS/PACKAGING SPECIFICATIONS

DIMENSIONS: mm	Bulk	Tape			
	Pcs/bag (typical)	Pcs/7 inch (178 mm) reel		Pcs/13 inch (330 mm) reel	
	Plastic	Paper	Embossed	Paper	Embossed
T : 1.25 $^{+0}_{-0.2}$	1000	N/A	1000	N/A	5000
T : 1.5 $^{+0}_{-0.2}$	1000	N/A	1000	N/A	5000
T : 2.0 $^{+0}_{-0.2}$	1000	N/A	1000	N/A	4000

HIGH DIELECTRIC CONSTANT TYPE Y5V



Note: Capacitance values = EIA 6 Step = 10, 15, 22, 33, 47, 68. For values not listed, contact your local Murata Erie Sales Office.

STANDARD THICKNESS/PACKAGING SPECIFICATIONS

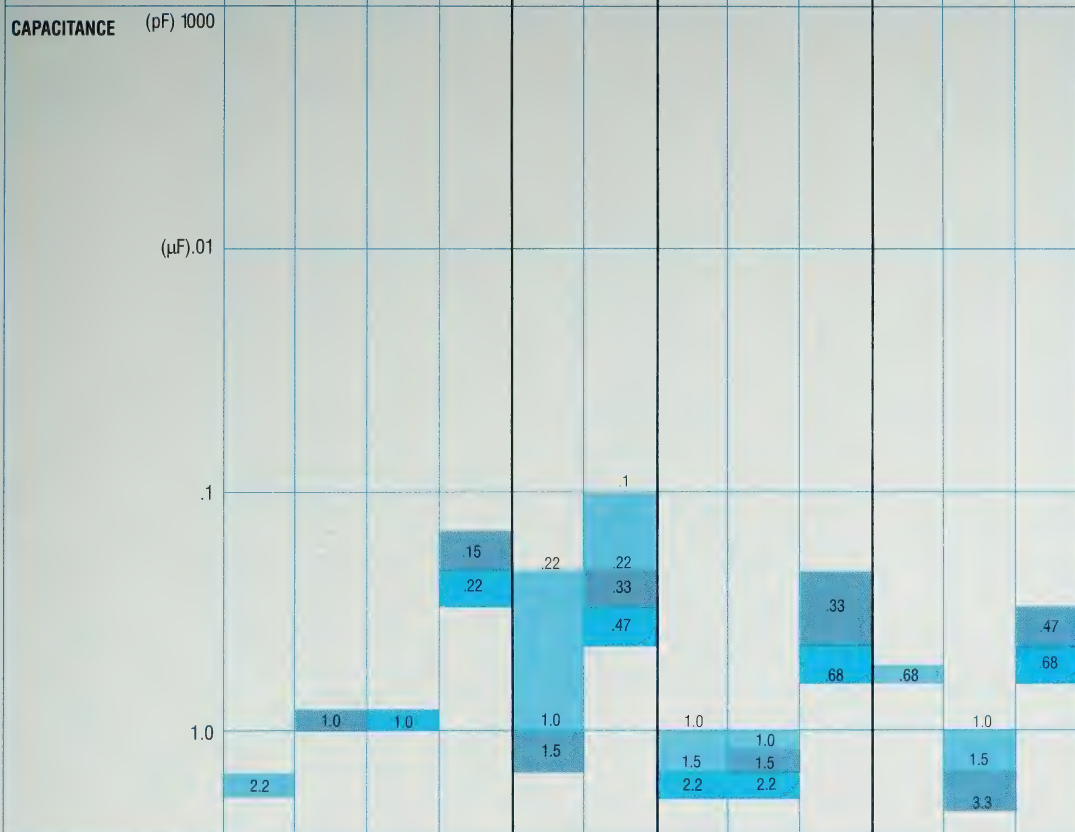
DIMENSIONS: mm	Bulk	Tape			
	Pcs/bag (typical)	Pcs/7 inch (178 mm) reel		Pcs/13 inch (330 mm) reel	
	Plastic	Paper	Embossed	Paper	Embossed
T : 0.7 $^{+0}_{-0.2}$	1000	4000	4000	10000	10000
T : 0.8 ±0.1	1000	4000	N/A	10000	N/A
T : 1.0 $^{+0}_{-0.2}$	1000	4000	3000	10000	10000
T : 1.25 $^{+0}_{-0.2}$ *	1000	N/A	3000	N/A	10000
T : 1.5 $^{+0}_{-0.2}$	1000	N/A	2000	N/A	8000

*GRM40 T = 1.25 ± .1

muRata ERIE

HIGH DIELECTRIC CONSTANT TYPE Y5V

MURATA ERIE DESIGNATION	GRM 43-2				GRM 43-4		GRM 44-1			GRM 44		
EIA TYPE DESIGNATION	1812				1825		2220			2225		
WVDC	16	25	50	100	50	100	25	50	100	25	50	100



Note: Capacitance values = EIA 6 Step = 10, 15, 22, 33, 47, 68. For values not listed, contact your local Murata Erie Sales Office.

STANDARD THICKNESS/PACKAGING SPECIFICATIONS

DIMENSIONS: mm	Bulk	Tape			
	Pcs/bag (typical)	Pcs/7 inch (178 mm) reel		Pcs/13 inch (330 mm) reel	
	Plastic	Paper	Embossed	Paper	Embossed
T : $1.25^{+0}_{-0.2}$	1000	N/A	1000	N/A	5000
T : $1.5^{+0}_{-0.2}$	1000	N/A	1000	N/A	5000
T : $2.0^{+0}_{-0.2}$	1000	N/A	1000	N/A	4000

CHIPS–GRM Series
FOR LOW PROFILE AND SUB-PLCC
HIGH DIELECTRIC CONSTANT TYPE X7R, Y5V

MURATA ERIE DESIGNATION	GRM 40-024						GRM 40-037						GRM 40-026					
EIA TYPE DESIGNATION	0805						0805						0805					
MAX THICKNESS	.020						.026						.028					
WVDC	16		25		50		16		25		50		16		25		50	
TEMPERATURE CHARACTERISTIC	X7R	Y5V	X7R	Y5V	X7R	Y5V	X7R	Y5V	X7R	Y5V	X7R	Y5V	X7R	Y5V	X7R	Y5V	X7R	Y5V
CAPACITANCE (pF) 100 – 1000 – .01(µF) – .1 – 1.0	.01 – .027	.047 – .1	2200 – .01	2200 – .033	220 – 6800	1000 – .01	.033 – .056	.15 – .22	.015 – .022	.056 – .1	.01 – .018	.027 – .047	.033 – .047	.15	.015 – .022	.1	.012 – .015	.033 – .047

PACKAGING = Bulk 1,000 pcs/bag **TAPE AND REEL:** 4,000 pcs/7" (178mm) Reel, 10,000 pcs/13" (330mm) Reel **Paper tape only.**

Note: For X7R, Capacitance values = E1A 12 Step = 10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82.
For Z5U and Y5V, Capacitance values = E1A 6 Step = 10, 15, 22, 33, 47, 68.
For values not listed, please contact your local Murata Erie Sales Office.

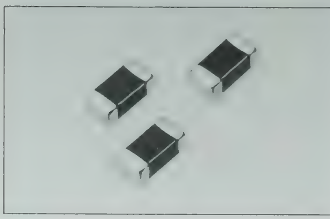
FOR LOW PROFILE AND SUB-PLCC
HIGH DIELECTRIC CONSTANT TYPE X7R, Z5U, Y5V

MURATA ERIE DESIGNATION	GRM 42-625				GRM 42-626		GRM 42-224				GRM 42-225				GRM 42-221			GRM 42-226		
EIA TYPE DESIGNATION	1206				1206		1210				1210				1210			1210		
MAXIMUM THICKNESS	.024				.028		.020				.024				.026			.028		
WVDC	16	25			16	25	16	25			16	25			25			25		
TEMPERATURE CHARACTERISTIC	Y5V	X7R	Z5U	Y5V	Y5V	Y5V	Y5V	X7R	Z5U	Y5V	Y5V	X7R	Z5U	Y5V	X7R	Z5U	Y5V	X7R	Z5U	Y5V
CAPACITANCE (pF) 100 – 1000 – .01(µF) – .1 – 1.0	.22	N/A	.1	.056 – .22	.33	.22	.47	.018 – .047	.1	.068 – .15	.47 – .68	1000 – .1	.022 – .15	.15 – .22	N/A	.22	N/A	.056 – .082	.22 – .33	.33

PACKAGING = Bulk: 1,000 pcs/bag **TAPE AND REEL:** 4,000 pcs/7" (178mm) Reel, 10,000 pcs/13" (330mm) Reel **Paper tape only.**

Note: For X7R, Capacitance values = E1A 12 Step = 10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82.
For Z5U and Y5V, Capacitance values = E1A 6 Step = 10, 15, 22, 33, 47, 68.

MLC CAPACITORS
TO REPLACE TANTALUMS AND ELECTROLYTICS



These new monolithic ceramic chip capacitors are specifically designed to replace tantalum and aluminum electrolytic capacitors in a variety of applications. The high frequency performance of these devices make them particularly suitable for use in secondary suppression circuits in switching power supplies and other circuits with high frequency performance requirements.

Lower ESR yields lower net impedance at higher frequencies. Thus a lower value of ceramic capacitance may be sufficient in bypassing and decoupling circuits.

Greater surface mounting flexibility and long-term reliability of ceramic capacitors adds to their overall performance vs. cost ratio as compared to electrolytics.

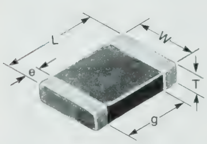
FEATURES*
- **Lower equivalent series resistance**
- **Lower dissipation factor**
- **Higher insulation resistance**
- **Higher break-down voltage**
- **No polarity considerations**
- **Long term dielectric stability**
- **Wider solder profile capability**
- **Solvent wash compatibility**

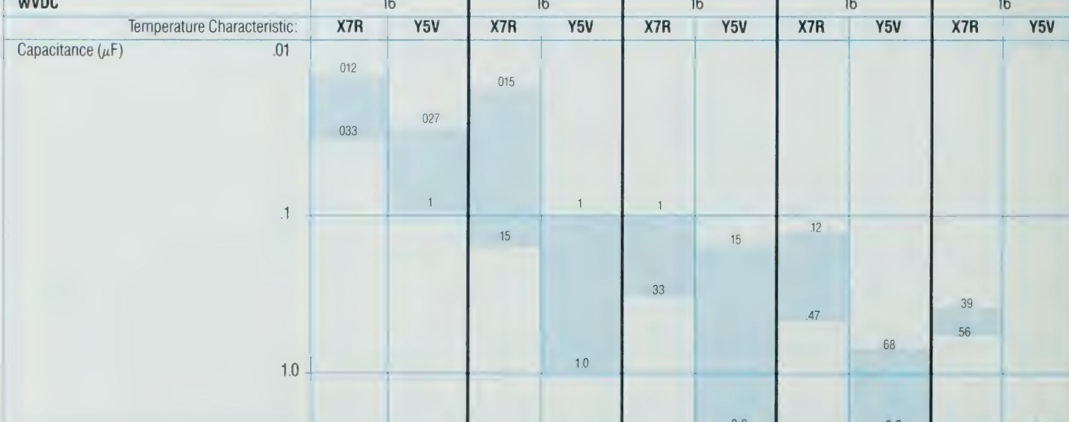
*When compared to electrolytic capacitors

BENEFITS*
- **Better high frequency performance**
- **Reduces loss, heat dissipation**
- **Lower power consumption**
- **Increased reliability**
  Less over-rating required
- **Eliminates insertion mistakes**
  Increases circuit design flexibility
  No D.C. bias voltage required
- **Reduces field failures—increases equipment life**
- **Greater surface mount flexibility and durability**

EIA Preferred Sizes—Nickel barrier terminations suitable for flow and reflow soldering

MURATA ERIE DESIGNATION		GRM39	GRM40	GRM42-6	GRM42-2	GRM43-2
EIA TYPE DESIGNATION		0603	0805	1206	1210	1812
DIMENSIONS: in. (mm)	L	.060±.008 (1.5±0.2)	.080±.008 (2.0±0.2)	.125±.008 (3.2±0.2)	.125±.008 (3.2±0.2)	.180±.012 (4.6±0.3)
	W	.030±.008 (0.75±0.2)	.050±.008 (1.25±0.2)	.060±.008 (1.5±0.2)	.100±.008 (2.5±0.2)	.125±.008 (3.2±0.2)
	T max.	.035 (0.9)	.053 (1.35)	.060 (1.5)	.060 (1.5)	.080 (2.0)
	g min	.020 (0.5)	.030 (0.75)	.040 (1.0)	.040 (1.0)	.080 (2.0)
	e	.014±.006 (0.35±0.2)	.020±.010 (0.5±0.25)	.020±.010 (0.5±0.25)	.020±.010 (0.5±0.25)	.025±.015 (0.63±0.38)
WVDC		16	16	16	16	16





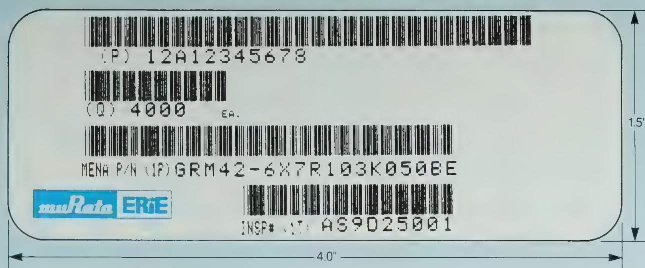
Note: For X7R, Capacitance values = E1A 12 Step = 10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82.
For Z5U and Y5V, Capacitance values = E1A 6 Step = 10, 15, 22, 33, 47, 68.
For values not listed, please contact your local Murata Erie Sales Office.

STANDARD BAR CODE FORMAT AND SPECIFICATIONS

MENA STANDARD INNER PACKAGE LABEL

CODE KEY

Customer Part Number
Quantity
MENA Part Number
Lot/Inspection Number

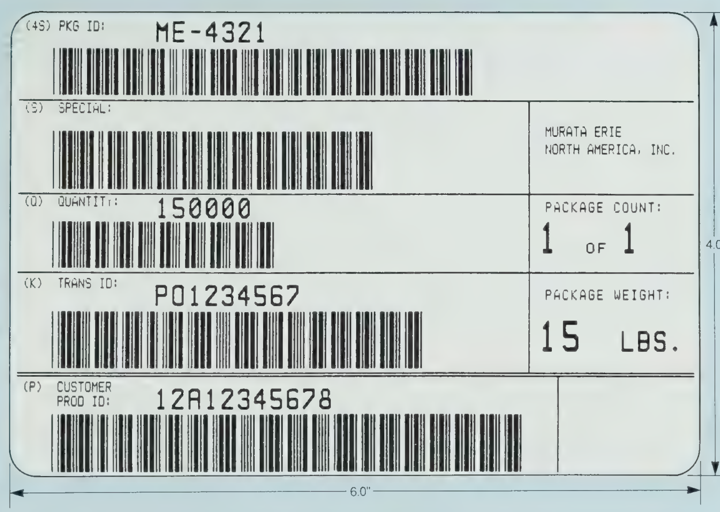


DIMENSIONS: inches

MENA STANDARD SHIPPING LABEL EIA-556 FORMAT

CODE KEY

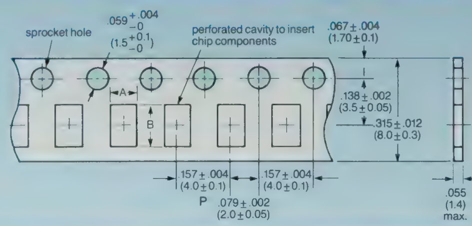
Supplier/Pkg. I.D.
Special
Quantity
Transaction ID (P.O.)
Customer Product ID (No.)



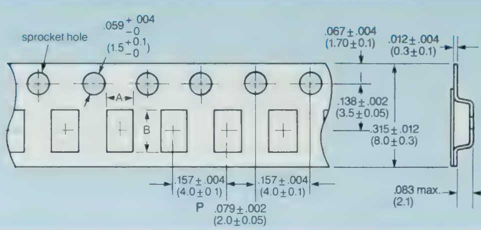
DIMENSIONS: inches

CHIPS–GRM SERIES
TAPE CARRIER DIMENSIONS

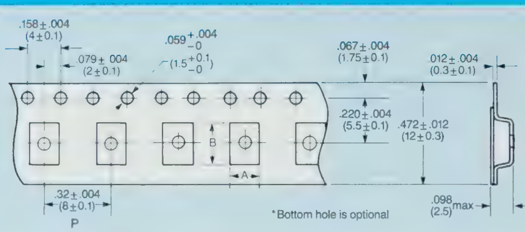
DIMENSIONS: In. (mm)



8mm PUNCHED (PAPER)	GRM39 0603	GRM40 0805	GRM42-6 1206	GRM42-2 1210
Tape A max.	.047 (1.2)	.065 (1.65)	.087 (2.2)	.116 (2.95)
Tape B max.	.079 (2.0)	.095 (2.4)	.150 (3.8)	.144 (3.65)
Chip T max.	.035 (0.9)	.040 (1.0)	.040 (1.0)	.040 (1.0)
Tape Pitch: P	.157±.004 (4.0±0.1)	.157±.004 (4.0±0.1)	.157±.004 (4.0±0.1)	.157±.004 (4.0±0.1)

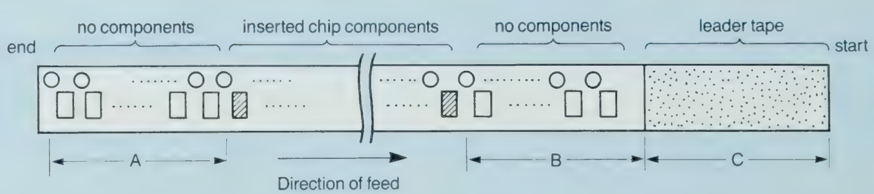


8mm EMBOSSED (PLASTIC)		GRM40 0805	GRM42-6 1206	GRM42-2 1210
Tape A max.		.061 (1.55)	.079 (2.0)	.114 (2.9)
Tape B max.	N/A	.093 (2.35)	.142 (3.6)	.142 (3.6)
Chip T max.		.053 (1.35)	.060 (1.5)	.060 (1.5)
Tape Pitch: P		.157±.004 (4.0±0.1)	.157±.004 (4.0±0.1)	.157±.004 (4.0±0.1)



12mm EMBOSSED (PLASTIC)	GRM43-2 1812	GRM43-4 1825	GRM44-1 2220	GRM44 2225
Tape A max.	.146 (3.7)	.197 (5.0)	.209 (5.3)	.264 (6.7)
Tape B max.	.197 (5.0)	.268 (6.8)	.244 (6.2)	.248 (6.3)
Chip T max.	.080 (2.0)	.080 (2.0)	.080 (2.0)	.080 (2.0)
Tape Pitch: P	.320±.004 (8±0.1)	.320±.004 (8±0.1)	.320±.004 (8±0.1)	.320±.004 (8±0.1)

TAIL AND LEADER TAPE DIMENSIONS: in. (mm)



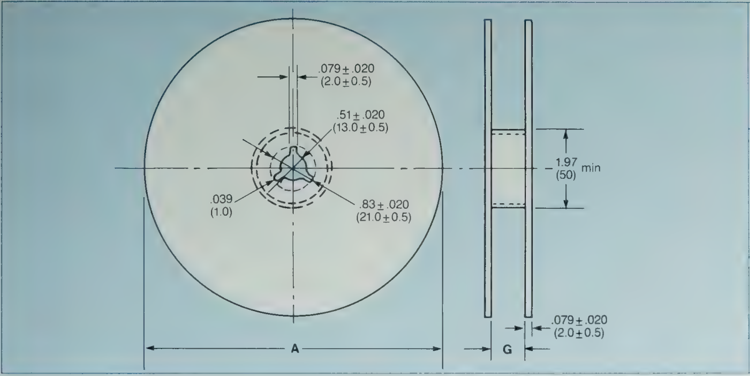
	Tail Tape (A)	Empty Cavities (B)	Leader Tape (C)
EIA-481-1	6.3 to 8.2 (160 to 200)	6.3 to 7.4 (160 to 188)*	9.0 to 9.8 (230 to 250)

*20 to 30mm must be unsealed with remaining portion of empty cavities sealed.

muRata ERIE

REEL DIMENSIONS & MARKING SPECIFICATIONS

REEL DIMENSIONS: in (mm)



Reel Diameter A	Width of Tape Carrier G	
	For 8mm Tape	For 12mm Tape
7±.079 (178±2.0)	$.331^{+.069}_{-0}$ ($8.4^{+1.5}_{-0}$)	$.488^{+.076}_{-0}$ ($12.4^{+2.0}_{0}$)
13±.079 (330±2.0)		

CHIP MARKING SPECIFICATIONS

Alphabetic Character	Significant Figures	Alphabetic Character	Significant Figures	Alphabetic Character	Significant Figures
A	1.0	M	3.0	Y	8.2
B	1.1	N	3.3	Z	9.1
C	1.2	P	3.6	a	2.5
D	1.3	Q	3.9	b	3.5
E	1.5	R	4.3	d	4.0
F	1.6	S	4.7	e	4.5
G	1.8	T	5.1	f	5.0
H	2.0	U	5.6	m	6.0
J	2.2	V	6.2	n	7.0
K	2.4	W	6.8	t	8.0
L	2.7	X	7.5	y	9.0

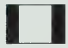
Numeric Character	Decimal Multiplier
0	10^0
1	10^1
2	10^2
3	10^3
4	10^4
5	10^5
6	10^6
7	10^7
8	10^8
9	10^{-1}

MARKING

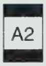
1. The capacitance value is expressed in pF.
2. A two character marking system will be used. The first character will be an alphabetic symbol and it will designate the 1st and 2nd figures of capacitance. The second character will be a numerical digit and it will designate the decimal multiplier of capacitance.

   Examples: A1 = 1 × 10^1 = 10pF
   J5 = 2.2 × 10^5 = 0.22μF
3. The marking shall appear in black or legible contrast. The orientation of the marking shall be as illustrated.
4. Marking resistance to solvents per EIA-RS-198 Method 210.

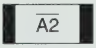
GRM39
No Marking



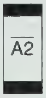
GRM40



GRM42-6, 42-2,
43-2, 44-1, 44



GRM43-4

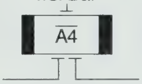


TC BAR CODE

Where chip marking is required, bar code designations for temperature coefficients (TC's) will be provided as listed below.

NPO=□□, N150=□□, N220=□□,
N330=□□, N470=□□, N750=□□,
Y5V=□□, Z5U=□□, X7R=|□□

Other TC Designators are available. Contact Factory.



STORAGE LIFE

Chip component terminations should generally be protected from moisture. In addition, they should also be protected from materials containing chlorine, sulfur compounds or any harmful gases that could cause degradation of the solder. Nylon-polyethylene laminated bags are used for both bulk and reel packaging. These special bags have been developed to keep out moisture and harmful gases. However, the following recommendations should be adhered to:

1. All chip components, including tape and reel, should be kept in sealed bags until they are used, where the temperature is less than 40°C and where the humidity is less than 70%.
2. The chip components should be used within six months after opening of the sealed bags they are furnished in.
3. The solderability of the chip components should be checked in the event that the bags are opened and not used for six months.
4. Peel strength and shelf life of tape are guaranteed for 1 year when stored under afore said conditions.

MECHANICAL CONSIDERATIONS

COEFFICIENTS OF THERMAL EXPANSION (CTE)

Generally, the most critical components in a surface mount assembly on P.C.B. materials are the ceramic capacitors and resistors. Other passive and active components, although surface mountable, generally have leads or electrodes which are compliant. Ceramic chip capacitors and resistors are leadless.

Mismatches in CTE's between chip and board material will cause stress. Ceramic capacitors with CTE's higher than board materials (i.e. alumina ceramic) will shrink more than the substrate when cooling after solder (above 200 +°C). Lead end termination bonding or ceramic defects can lead to mechanical failures. When chips are mounted on boards with higher CTE's, repeated temperature cycling can contribute to failures by:

- cracks in solder fillets
- cracks in ceramic components
- separation of terminations from chip bodies

Typical ceramic component CTE's are: (IN/IN/°C)

COG Chip Capacitor	$8{-}10 \times 10^{-6}$
X7R Chip Capacitor	$11{-}12 \times 10^{-6}$
Z5U Chip Capacitor	$11{-}12 \times 10^{-6}$
Recommended Expansion Ratio of P.C.B.:	$3{-}16 \times 10^{-6}$

The recommended P.C.B. expansion ratio accounts for chip terminations which absorb a portion of the thermal stress mismatch.

The chip components mounting pad or land should be designed to provide for an electrically and mechanically solid solder joint.

Land dimensions are generally determined by the size of the chips, placement accuracy and the amount of solder necessary to create a solid joint.

In particular, the ability of chips to withstand mechanical stress such as board flex and temperature cycling is influenced by the amount of solder applied.

The larger the amount of solder applied to the bonding of the chips, the greater the mechanical stress on the chips. In fact, excess solder may cause the chips to crack.

In order to prevent such defects, it is first necessary to consider the size of lands. This in turn determines the amount of solder necessary to form the fillet.

In wave soldering, the soldering area is fully immersed in molten solder. This provides enough solder to form the fillet. However, in reflow soldering, the solder fillet is largely controlled by the amount of solder paste lay down. Therefore, it is recommended that reflow soldering lands be the same or slightly larger than those designed for wave soldering.

Recommended Land Dimensions (P.C.B.)

Pad dimensions are determined by the mounting requirements, the amount and type of solder system used and the placement technique.

Ceramic Chip Capacitors are susceptible to stresses when applied on P.C.B. materials. Recommended pad dimensions are indicated.

Actual pad dimensions, within the specified range, will depend upon the type of assembly and soldering system employed:

Wave or Flow Soldering (with adhesive bonding) – Optimum pad width (c) is designated as ²/₃ of the chip width (W). Pads larger than the chip width can lead to three (3) potential problems due to stress transfer:

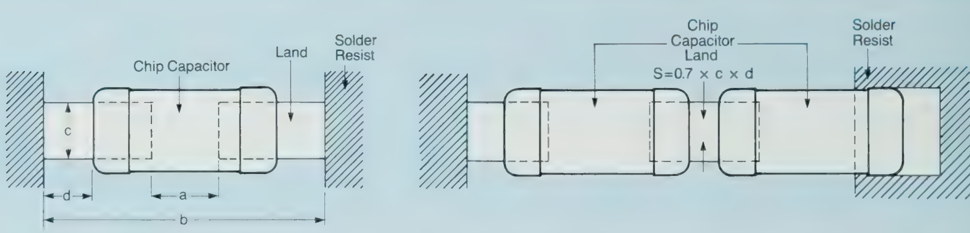
- peel away of chip end termination
- cracks in solder fillet
- cracks in ceramic chip

Stresses are more evenly transferred during wave solder by maintaining pad width as ²/₃ width of chip.

Reflow or Vapor Phase Soldering (with solder paste) – Optimum pad is designated as the exact width of the chip.

Pad dimensions for all Murata Erie chip components are indicated. Adherence to these guidelines will improve the solderability success rate and minimize component movement.

CHIP MONOLITHIC CERAMIC CAPACITOR – GRM – PAD DIMENSIONS



MURATA ERIE DESIGNATION		REFLOW SOLDERING GRM39	GRM40	GRM42-6	GRM42-2	GRM43-2	GRM43-4	GRM44-1	GRM44	WAVE SOLDERING* GRM40	GRM42-6	GRM42-2
DIMENSIONS: in. (mm)	L	.060 ± .008 (1.5±0.2)	.080 ± .008 (2.0±0.2)	.125 ± .008 (3.2±0.2)	.125 ± .008 (3.2±0.2)	.180±.012 (4.6±0.3)	.180±.012 (4.6±0.3)	.220±.012 (5.6±0.3)	.220±.012 (5.6±0.3)	.080±.008 (2.0±0.2)	.125±.008 (3.2±0.2)	.125±.008 (3.2±0.2)
	W	.030±.008 (0.75±0.2)	.050±.008 (1.25±0.2)	.060±.008 (1.5±0.2)	.100±.008 (2.5±0.2)	.125±.008 (3.2±0.2)	.250±.016 (6.35±0.4)	.200 [illegible] (5.1 [illegible])	.250±.016 (6.35±0.4)	.050±.008 (1.25±0.2)	.060±.008 (1.5±0.2)	.100±.008 (2.5±0.2)
a		.016 to .039 (0.4 to 1.0)	.039 to .055 (1.0 to 1.4)	.071 to .098 (1.8 to 2.5)	.071 to .098 (1.8 to 2.5)	.098 to .138 (2.5 to 3.5)	.098 to .138 (2.5 to 3.5)	.106 to .201 (2.7 to 4.7)	.106 to .185 (2.7 to 4.7)	.039 to .055 (1.0 to 1.4)	.071 to .098 (1.8 to 2.5)	.071 to .098 (1.8 to 2.5)
b		.098 to .161 (2.5 to 4.1)	.118 to .181 (3.0 to 4.6)	.165 to .228 (4.2 to 5.8)	.165 to .228 (4.2 to 5.8)	.217 to .240 (5.5 to 6.1)	.217 to .240 (5.5 to 6.1)	.264 to .327 (6.7 to 8.3)	.264 to .327 (6.7 to 8.3)	.118 to .157 (3.0 to 4.0)	.165 to .205 (4.2 to 5.2)	.165 to .205 (4.2 to 5.2)
c		.024 to .039 (0.6 to 1.0)	.035 to .063 (0.9 to 1.6)	.047 to .079 (1.2 to 2.0)	.071 to .126 (1.8 to 3.2)	.091 to .165 (2.3 to 4.2)	.157 to .295 (4.0 to 7.5)	.138 to .256 (3.5 to 6.5)	.157 to .295 (4.0 to 7.5)	.035 to .047 (0.9 to 1.2)	.047 to .063 (1.2 to 1.6)	.071 to .098 (1.8 to 2.5)
d		.020 to .051 (0.5 to 1.3)	.020 to .051 (0.5 to 1.3)	.020 to .051 (0.5 to 1.3)	.020 to .051 (0.5 to 1.3)	.020 to .051 (0.5 to 1.3)	.020 to .051 (0.5 to 1.3)	.020 to .051 (0.5 to 1.3)	.020 to .051 (0.5 to 1.3)	.020 to .039 (0.5 to 1.0)	.020 to .039 (0.5 to 1.0)	.020 to .039 (0.5 to 1.0)

* Effective area of the land S should satisfy: $S \leqq c(MAX) \times d(MIN)$. c and d need not be within the range shown in this list.

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P.C.B. Pattern Configurations for Ceramic Chip Capacitors and Resistors for Wave Soldering

Pattern configurations and orientation of ceramic leadless components can affect the resultant fillet during wave solder.

Ideally, ceramic chip terminations should be aligned perpendicular to the direction of wave flow in an end to end or staggered end to end configuration:

In this case a pass through the wave from bottom to top or from top to bottom will deposit sufficient solder on both individual chip terminations resulting in acceptable fillets.

On P.C.B. layouts where ceramic chips are rotated 90° in relation to each other in a body—centered or space—centered pattern, potential soldering problems may occur.

A wave solder pass from top to bottom of the P.C.B. will result in acceptable solder fillets at the chip end terminations which are perpendicular (horizontal in the below depiction) to the direction of pass. However, adequate solder may not be deposited on the bottom termination of chips rotated 90° due to termination shadowing by the ceramic chip body. A cold joint could result.

Refinements have been incorporated in wave solder systems including dual waves where the first wave is turbulent and "forces" solder onto component terminations and pad areas. This equipment may reduce the incidence of cold joints in body centered board layouts.

P.C.B. layout and pattern configurations can affect solderability.

P.C.B. Deflection (Bending) and Ceramic Chip Capacitors and Resistors

All surface mount components, but in particular ceramic chip capacitors and resistors, are subject to the mechanical stresses generated during deflection or bending of the printed circuit board.

A test has been developed to establish the capacitors or resistors capability to withstand P.C.B. bending.

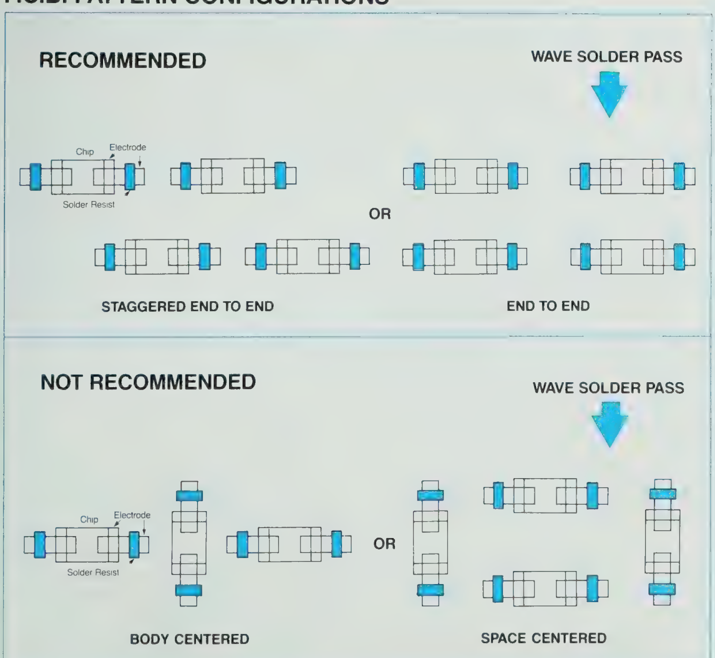
The capacitor or resistor is soldered onto the testing board with a eutectic solder. The soldering should be done with an iron or by reflow and should result in a uniform fillet with no thermal shock to the component. A stress is applied in order to depress the board at a rate of 0.5mm per second.

The component shall withstand deflection, dependent upon material of 2mm.

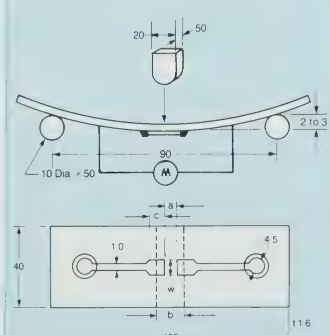
This guideline stresses the need for the user to exercise control in two areas:

1. Board warpage as received from the P.C.B. supplier
2. The amount of deflection the P.C.B. is subjected to after soldering

P.C.B. PATTERN CONFIGURATIONS



DIMENSIONS: in. (mm)



Size	Type	a	b	c	w
0805	GR40	.047 (1.2)	.157 (4.0)	.118 (3.0)	.065 (1.65)
1206	GR42-6	.087 (2.2)	.197 (5.0)	.098 (2.5)	.079 (2.0)

SOLDERING CONSIDERATIONS

Soldering of Passive Surface Mount Components

Surface mount passive components may be soldered to P.C.B.'s and substrates in a variety of methods:

- wave/dual wave
- hot air/convection reflow
- vapor phase reflow
- infrared reflow
- bubble solder immersion
- other (laser, etc.)

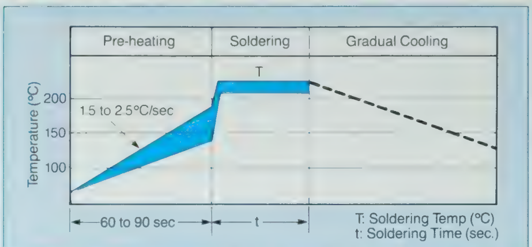
Ceramic devices, particularly chip capacitors and resistors, generally have a poor ability to withstand heat shock. Thermal shock may result during soldering and is a natural material characteristic. Chip capacitor failure mechanisms resulting from excessive thermal shock may include:

- micro cracks in the ceramic
- electrical shorts
- insulation resistance degradation in accelerated life test conditions

Users of ceramic chip components can minimize thermal shock by employing a basic process prior to soldering: *PREHEAT THE CERAMIC CHIP COMPONENTS AND BOARD TO WITHIN 100°C OF THE SOLDERING TEMPERATURE.* The time for preheat should be a minimum of one (1) minute.

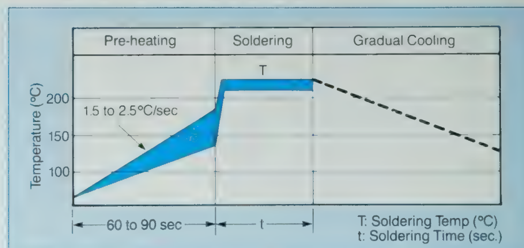
In addition, the recommended soldering process time-temperature profile for components should be followed.

WAVE SOLDERING



Product Name		Soldering Temp. T (°C)	Soldering Time t (sec.)
Chip Monolithic	GR	220 to 260°C	5 sec. max.
Ceramic Capacitor	GRM	220 to 260°C	10 sec. max.

INFRARED REFLOW SOLDERING



Product Name		Soldering Temp. T (°C)	Soldering Time t (sec.)
Chip Monolithic	GR	220 to 240°C	20 sec. max.
Ceramic Capacitor	GRM	220 to 250°C	30 sec. max.

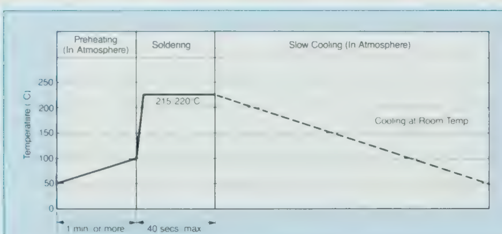
Note: For Sizes Greater Than 1210, Wave Soldering Not Recommended.

VAPOR PHASE REFLOW SOLDERING

Vapor phase reflow soldering techniques may be used to attach many surface mount components onto a P.C.B. or substrate at one time. Solder temperatures are controlled precisely due to the known boiling point of the liquid.

Vapor phase soldering involves condensation heating, whereby the latent heat of a vaporized liquid is released as the vapor condenses on metalization of the parts to be soldered. The phase change from liquid to vapor is rapid and occurs on all exposed surfaces of the part, resulting in uniform heating.

Murata Erie surface mount components can be successfully attached to a P.C.B. or substrate using the vapor phase reflow technique. Due to the lower soldering temperature, the effect of heat on the components is not severe.



Primary liquid

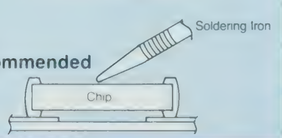
Product Name		Maker	Boiling Point
Fluorinert	FC-70	3M	215°C
Fluorinert	FC-5311		215°C
Galden	LS/215	Montedison	215±3°C
Galden	LS/230	S.P.A.	230±5°C

Secondary liquid
Trichlorotrifluoroethane—Boiling point 48°C

SOLDERING IRON

Recommended

Not Recommended



The soldering iron method is used primarily for rework or breadboarding. It is important that the solder iron tip *not touch* the ceramic component body. The iron should be applied only to the termination—solder fillet.

Note: The soldering iron shall be of the nichrome wire heater type with maximum tip diameter of 3.0mm.

Product Name		Soldering Iron Tip Temp.	Soldering Time	Iron Output
Chip Monolithic Ceramic Capacitor	GR	280°C max.	5 sec. max.	30W max.
	GRM		10 sec. max.	

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RECOMMENDED FLUX AND SOLDER

Flux: Use a resin-based flux, however, do not use a strong acidic flux where the chlorine content exceeds 0.20%.

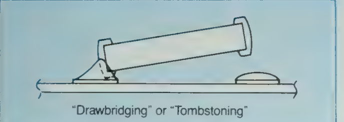
Solder: Eutectic solder or 6 × 4 solder should be used for all components, except GR, where 6 × 4 solder containing 2 to 2.5% silver should be used.

RECOMMENDED CLEANING CONDITIONS

Product Name		Cleaning Liquid	Immersion Cleaning	Ultrasonic Cleaning
Chip Monolithic Ceramic Capacitor	GR GRM	Freon Chlorosen Isopropyl alcohol	5 min. max.	1 min. max.

"DRAWBRIDGING" OR "TOMBSTONING"

refers to the tendency of a chip capacitor or resistor to stand on end during the solder process:



"Drawbridging" or "Tombstoning"

This phenomenon is caused by the relief of surface tension forces during solder wetting.

An example is the failure to properly wet each chip end termination equally or at the same time. One end of the chip is raised above the pad and fails to bond to the land area.

Factors which contribute to "drawbridging" include:

A. Improper Pad or Land Design:
Unequal pad sizes for individual chips may result in the chip standing on end on the larger pad.

B. Improper or Unequal Solder on Pads:
A larger solder mass on one chip pad will also cause the chip to stand on end.

C. Misplacement of Chip:
If one component end termination is placed in solder paste and the other termination is not, the "pasted" end will stand up.

D. Poor Chip End Termination:
Component suppliers must evenly and equally control the termination on individual chips. One larger termination on a single chip can lead to "tombstoning."

E. Vibration of Chip Loaded P.C.B.'s Prior to Soldering:
P.C.B.'s with components mounted but not soldered must be handled carefully to not jar and move components.

F. Poor Quality Solder Paste:
Is a problem with surface mount and leaded assemblies. Compatible and high quality materials should be chosen.

G. Improper Solder Temperature:
Excessive and uneven temperature excursions as well as extended dwell times can detrimentally effect solderability and contribute to "drawbridging." Recommended soldering conditions should be followed.

The use of proper design guidelines and materials will minimize chip "drawbridging" and "tombstoning."

THE USE OF ADHESIVES

Bonding chips temporarily to the P.C.B. prior to wave soldering is used extensively in double sided board assembly with underside mounted chip capacitors and resistors.

It is necessary to control the amount of adhesive so that it does not interfere with chip termination and pad contact area and does not bridge between P.C.B. component pads.

The recommended adhesive pattern for 1206 size chips is shown.

A non-conductive, heat cure epoxy resin adhesive with maximum viscosity (10,000 cps or greater) is recommended. Chips should be mounted within 15 minutes of adhesive printing. A U.V. cure of the adhesive after chip placement is common.

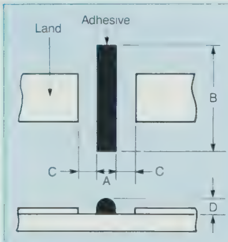
Notes Concerning Adhesive Application

Adhesive that is supplied on the substrate tends to spread out and decrease in thickness. It is necessary to keep adhesive thickness constant.

In the case where there is insufficient adhesion, the chip components are apt to fall from the substrate during flow soldering.

Amount of adhesive

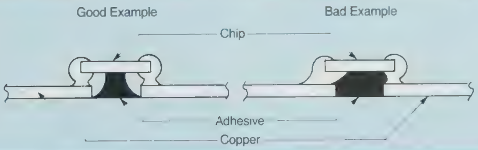
The proper amount of adhesive required depends on the size of the chip component.



Example: Chip Monolithic Ceramic Capacitors

		GR(M)40	GR(M)42-6	GR(M)42-2
Dimension	L	2.0	3.2	3.2
	W	1.25	1.6	2.5
A		0.6	0.8	0.8
B		1.8	2.1	3.0
C		0.3 min.	0.3 min.	0.3 min.
D		0.12±0.02	0.12±0.02	0.12±0.02

Unit: mm



In the case where too much adhesive is applied, the adhesive is apt to flow onto the lands, which results in bad soldering.

Required Characteristics for Adhesive

The adhesive should be suitable for dispenser use.

After application to the substrate, the adhesive should not spread out excessively.

The adhesive should be strong enough to firmly hold the components despite the vibrations of the machine during mounting.

The adhesive should have sufficient strength at high temperatures.

The adhesive should have excellent insulation and humidity resistance.

SOLDERING CONSIDERATIONS

Chip Ceramic Capacitor End Terminations

The standard chip ceramic capacitor end termination has been palladium silver.

This termination system has good but limited capabilities to withstand various soldering techniques.

Historically, there have been two (2) primary problems associated with the palladium silver termination:

1. Silver leaching or removal from the termination due to high solder temperature excursions and/or long solder dwell times.
2. Silver dendrite growth across the external surface of small chip capacitors due to voltage and/or humidity conditions

These problems have resulted in the development of a barrier layer end termination (GRM Series) consisting of three (3) layers:

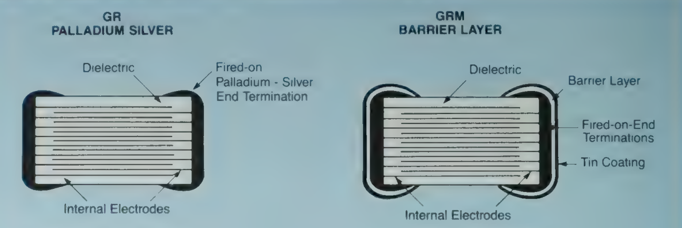
- palladium silver inner layer
- nickel barrier layer (plated)
- outer tin layer (plated)

Final chip dimensions are identical to the GR palladium silver termination series. Both chips are available in tape and reel for automatic placement.

The barrier layer termination is superior in soldering performance to the palladium silver termination, and has become the industry standard.

As an example, during wave soldering the 260°C, 3 to 5 second dwell recommended for the palladium silver termination can be increased to 35 to 40 seconds for the barrier layer termination.

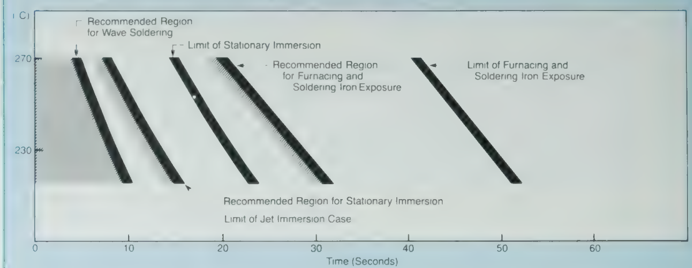
The barrier layer termination GRM series is ideally suited for customers manufacturing a multitude of products utilizing vairous solder techniques or for customers who do not closely control the time temperature profile of the soldering process. Leaching of silver during soldering may be eliminated.



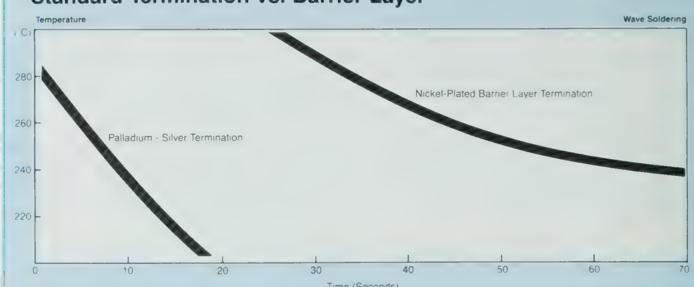
CUTAWAY CHIP CERAMIC CAPACITOR MURATA ERIE GR SERIES

CUTAWAY CHIP CERAMIC CAPACITOR MURATA ERIE GRM SERIES

Recommended Soldering Time — Temperature Profile Standard Palladium Silver End Termination



Silver Corrosion Time and Soldering Temperature Standard Termination vs. Barrier Layer



SOLDER MASS CONTROL

Ceramic chip capacitors and resistors, as noted previously, are susceptible to thermal and mechanical stresses when mounted on printed circuit boards.

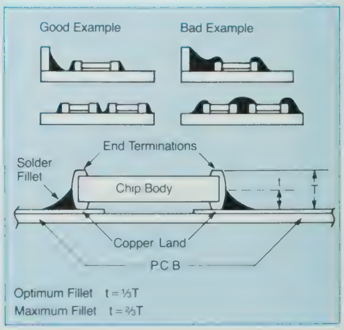
In an assembly operation which screen prints solder paste on land areas of the P.C.B., it is necessary to control the amount of solder paste to allow for adequate transfer of thermal and mechanical stresses from board to ceramic passive components.

In general, the solder mass should be controlled to result in a maximum fillet of 2/3 the overall thickness of the chip capacitor or resistor.

Larger fillets which extend above the component end terminations potentially can contribute to failure by:

- Peel-away of the end termination
- Fillet weld cracks at the top corners
- Cracks in the ceramic chip

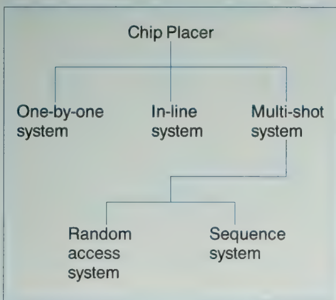
These problems can be minimized by adhering to the "2/3" design guideline for solder mass. (See example)



AUTOMATIC PLACEMENT EQUIPMENT CONSIDERATIONS

muRata ERiE

Classification of Chip Placers
There are various chip placers on the market today and are classified into three systems: One-by-one, In-line and Multi-shot.



SYSTEM FEATURES

One-by-one system
This system places chip components one-by-one on PCB's. It is suitable for both small-lot production requiring product change-over and for mid-scale mass-production. This system is the most popular.

In-line system
This system places chip components continuously using multiple placing heads. Placing speed is higher than the one-by-one system because of its simultaneous placing capability. This system is suitable for production of PCB's with few chip components.

Multi-shot system
This system places many chip components at the same time on a PCB. Placing speed per component is the highest for available machinery. This system is suitable for mass-production of large quantities of the same product. Components are restricted in size, such as to chip ceramic capacitors, resistors and SOT's.

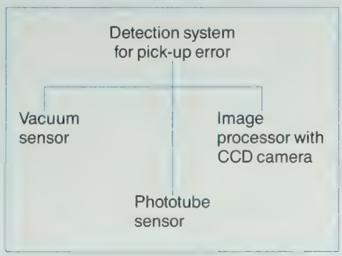
PLACING SPEED

One-by-one system
Placing speed differs due to dimensions and figures of components. Placing speed (in case of high speed type that can place from small to relatively large size chip components) is 0.2 to 0.4 seconds per component. Placing speed (in case of type that can place all chip components including SOIC) is 0.6 to a few seconds per component.

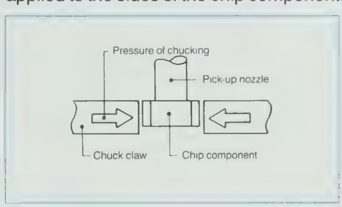
In-line system
Although placing speed by individual heads is low, placing speed per component is the same speed as that of high speed type one-by-one system. This is due to the placement of chip components at the same time using multiple placing heads.

Multi-shot system
Placing speed is 5-20 seconds per PCB. Though placing speed per component differs, it is 0.025-0.1 seconds per component in case of 200 components on one PCB.

Machine Detection System for Chip Components
Detecting systems are mainly of two types: vacuum sensor and phototube sensor. Phototube sensors have become the preferred method to easily detect pick-up error (such as a component picked up vertically). There is also a newer system which uses an image processor with a CCD camera.



Positioning System of Chip Components
Chip placers (one-by-one and in-line) generally have chuck claws for positioning chip components. Multi-system placers have plate-like jigs for positioning. In case of one-by-one and in-line systems, normally several to 300 grams of pressure is applied to the sides of the chip component.

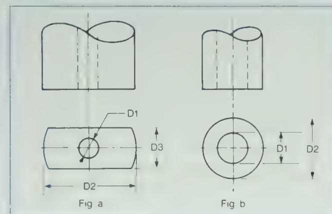


Cautions for Chip Placing
1. Prevention of PCB Warping. If there is a large warp in the PCB, there will be splitting, cracking or other damage to the chip components. It is necessary to prevent these defects by setting back-up pins under the PCB and holding close tolerance on board warpage.

2. Adjustment of Lower-Limit Point of Pick-up Nozzle. Usually 100-300 grams is applied by the pick-up nozzle to the top of the chip component during placing. If placing pressure is greater, there will be damage to the chip depending on chip type. It is necessary to prevent defects by adjusting the lower-limit point of the pick-up nozzle.

PICK AND PLACE HEAD

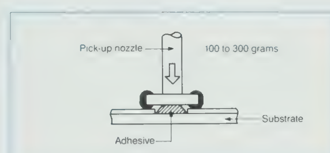
Pick-up nozzle size of chip placer
For small size chip components, a small pick-up nozzle is used. For larger chip components, a large pick-up nozzle is used. Examples of typical pick-up nozzle dimensions used are shown below.



		D1	D2	D3
Small size chip components for 8mm width tape	Fig. b	0.7	1.8	—
	Fig. a	1.3	2.4	1.6
	Fig. b	0.8	1.8	—
	Fig. b	1.0	1.8	—
	Fig. b	1.0	2.5	—
Large size chip components for 12mm width tapes	Fig. a	1.3	2.8	1.6
	Fig. a	1.8	4.5	2.6
	Fig. b	2.0	4.0	—

PLACEMENT PRESSURE

100 to 300 grams of pressure is applied to the surface of the chip component by the pick-up nozzle. Breakage of chip component may occur if the placement pressure is not properly adjusted.

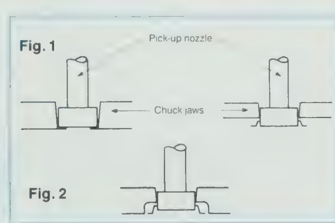


CHUCK JAWS

Generally, chuck jaws are shaped like those shown in Fig. 1. However, for chip components which have terminals that are bent outward, chuck jaws such as those shown in Fig. 2 are more appropriate. Chip components with outward bent terminals cannot be aligned properly by chuck jaws as shown in Fig. 1.

CHUCKING PRESSURE

Usually 100 to 300 grams of pressure is applied to the sides of the chip component.



MONOLITHIC CERAMIC CAPACITOR TO REPLACE ALUMINUM ELECTROLYTICS

RPE 210-260

FEATURES

- **High long term reliability (10 to 20 years)**
- **Non-polarized**
- **Increased high frequency performance reduces total capacitance requirements for equivalent impedance**
- **Epoxy coating meets UL94V-0**

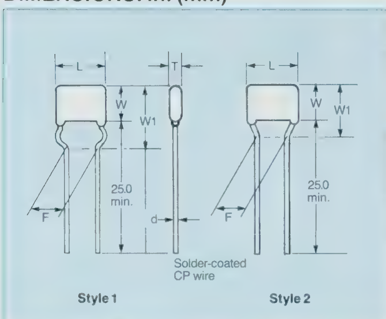
These new monolithic ceramic capacitors are specifically designed to replace aluminum electrolytic capacitors in a variety of applications. The high frequency performance of these devices makes them particularly suitable for use in secondary suppression circuits in switching power supplies and other circuits with high frequency performance requirements.

PART NUMBERING SYSTEM

RPE230 Z5U 106 Z 050V

- RPE230 — Type
- Z5U — Temperature Characteristics
- 106 — Nominal Capacitance
- Z — Capacitance Tolerance
- 050V — Rated Voltage

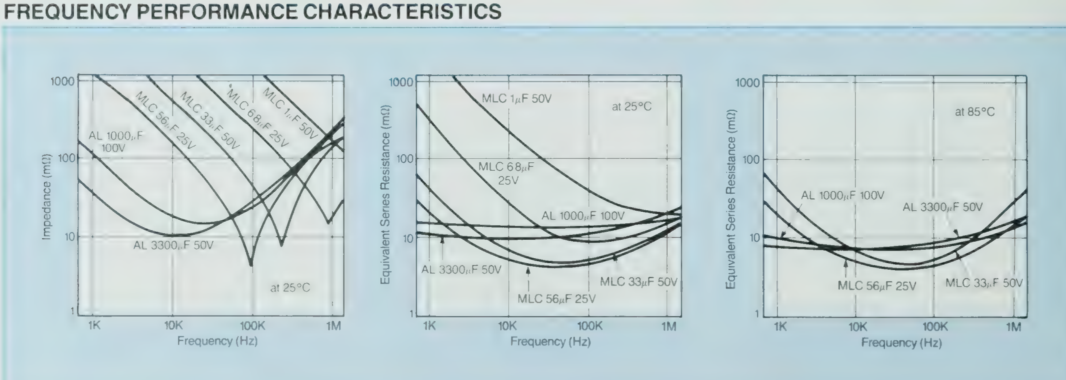
DIMENSIONS: in. (mm)



CAPACITANCE RANGE (μF)

Part Number	Rated Voltage, Nom. Cap. (μF) 25VDC	50VDC	75VDC	100VDC	Dimension (mm) W1 max.	L	T max.	F	d	Lead Style
RPE210	2.2–4.7	1.5, 2.2	—	1.0	10.0	7.5	4.0	5.0±0.8	0.6±0.05	1
RPE220	6.8	3.3, 4.7	—	1.5, 2.2	12.0	10.0	4.0	5.0±0.8	0.6±0.05	2
RPE230	—	6.8, 10	—	3.3, 4.7	15.0	12.5	5.0	10.0±0.8	$0.6^{+0.06}_{-0.05}$	1
RPE240	15	—	—	—	17.5	17.5	5.0	15.0±0.8	$0.8^{+0.06}_{-0.05}$	1
RPE250	22, 33, 47	15, 22	6.8, 10	—	18.0	24.0	7.5	15.0±0.8	$0.8^{+0.08}_{-0.05}$	2
RPE260	68, 100	33, 47	15, 22	—	21.0	35.0	7.5	25.4±1.5	$0.8^{+0.08}_{-0.05}$	2

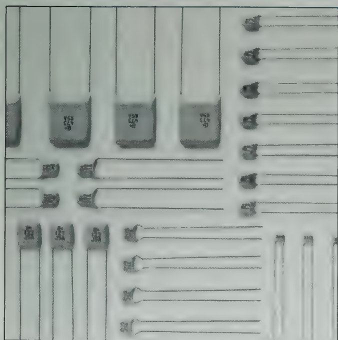
FREQUENCY PERFORMANCE CHARACTERISTICS



CONFORMAL COATED RADIAL LEADS

muRata ERIE

RPE 110-123



FEATURES:
- Wide capacitance, T.C., voltage and tolerance range
- Industry standard sizes
- Tape and Reel available for auto insertion
- Various lead spacing available
- Marking standard or to customer specification
- Epoxy coating meets UL94V-0

PART NUMBERING SYSTEM

RPE110-XXX X7R 103 K 050V

CAPACITOR TYPE AND SIZE

Used only for tape and reel and other variations. See pages 44-45.

TEMPERATURE CHARACTERISTICS (Note 3)
COG=0 ±30ppm (Notes 1 & 2)
X7R=±15%
Z5U=+22, −56%
Y5V=+22, −82%
(See Note 2 below)
P2H=N150±60ppm
R2H=N220±60ppm
S2H=N330±60ppm
T2H=N470±60ppm
U2J=N750±120ppm

CAPACITANCE VALUE
Expressed in picofarads and identified by a three-digit number. First two digits represent significant figures. Last digit specifies the number of zeros to follow. For values below 10pF, the letter "R" is used as the decimal point and the last digit becomes significant.

CAPACITANCE TOLERANCE (Note 2)
COG: (10pF or less)
B=±.1pF
C=±.25pF
D=±.5pF
F=±1pF
(over 10pF)
G=±2%
J=±5%
K=±10%
X7R: K=±10%
M=±20%
J=±5% on special request
Z5U: M=±20%
Z=+80, −20%
Y5V: Z=+80, −20%

VOLTAGE
Identified by a three digit number.
50 and 100V standard (200V and 500V on special request)

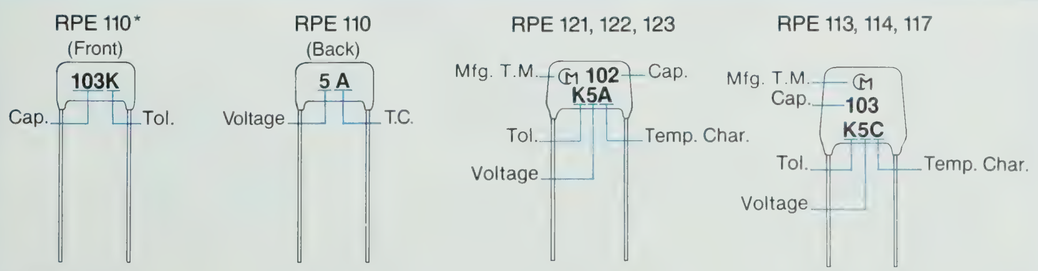
NOTES: T.C. Tolerance

Capacitance (pF)	T.C. Tolerance (ppm)
10 or over	± 30 (G)
4.0-9.9	± 60 (H)
2.1-3.9	±120 (J)
.4-2.0	±250 (K)

Refer to EIA RS-198 for limitations.

2. Refer to EIA-RS-198 for limitations.

MARKINGS



Voltage Code
2=25V, 5=50V,
1=100V, 6=200V, 9=500V

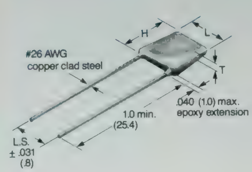
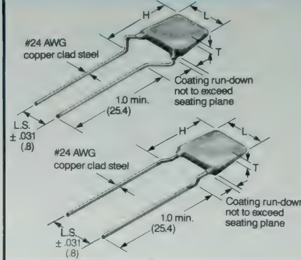
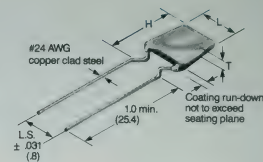
RPE 110: Cap. and Tol. only for X7R, Z5U and Y5V materials.

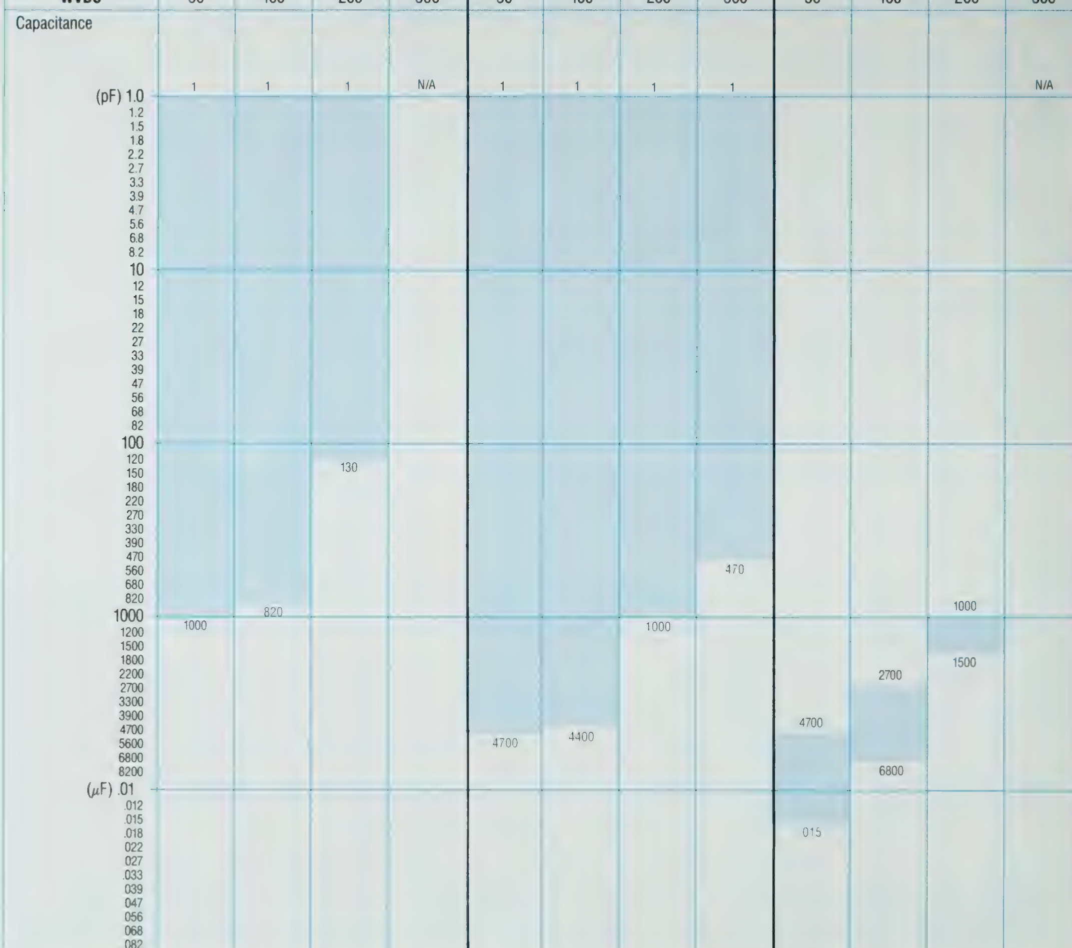
*Both sides marked for temperature compensating RPE 110 capacitors

Temp. Char. Code
A=COG, P=P2H, R=R2H, S=S2H, T=T2H, U=U2J, C=X7R, E=Z5U, F=Y5V

CONFORMAL COATED RADIAL LEADS
RPE Series

COG

DIMENSIONS: in. (mm)												
												
MURATA ERIE DESIGNATION	**RPE 110**				**RPE 121/RPE 122**				**RPE 123**			
L	.138 (3.5)				.200 (5.1)				.300 (7.6)			
H	.120 (3.1)				.250 (6.4)				.275 (7.0)			
T	.100 (2.5)				.125 (3.2)				.125 (3.2)			
L.S.	.100 (2.5)				.100 (2.5) / .200 (5.1)				.200 (5.1)			
WVDC	50	100	200	500	50	100	200	500	50	100	200	500
Capacitance	1 – 1000	1 – 820	1 – 130	N/A	1 – 4700	1 – 4400	1 – 1000	1 – 470	4700 – .015	2700 – 6800	1000 – 1500	N/A



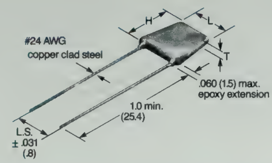
Note: Other values are available below 10pF. For requirements not shown, please contact your local Murata Erie Sales Office.

RPE Series

muRata ERIE

COG

DIMENSIONS:
in. (mm)



Standard package and lead configurations shown. Other variations and tape and reel data are displayed on pages 44-45. All RPE wire is tinned copper clad steel wire. For other requirements, please contact your local sales office.

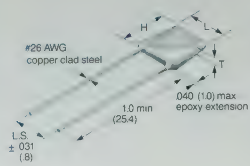
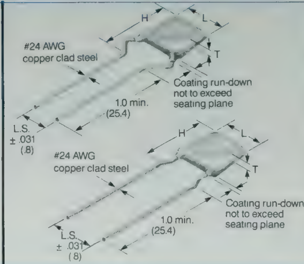
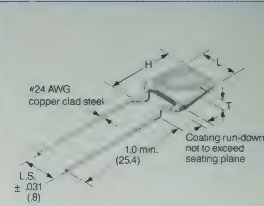
MURATA ERIE DESIGNATION	RPE 113				RPE 114				RPE 117			
L	.300 (7.6)				.400 (10.2)				.500 (12.7)			
H	.300 (7.6)				.400 (10.2)				.500 (12.7)			
T	.157 (4.0)				.157 (4.0)				.200 (5.1)			
L.S.	.200 (5.1)				.200 (5.1)				.400 (10.2)			
WVDC	50	100	200	500	50	100	200	500	50	100	200	500
Capacitance	1200	1200	560	270	.015	.015	3900	820	.027	022	.01	1300
	.018	012	3900	1500	.033	.033	.01	2200	.068	.056	027	6200

Capacitance scale: (pF) 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2, 10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82, 100, 120, 150, 180, 220, 270, 330, 390, 470, 560, 680, 820, 1000, 1200, 1500, 1800, 2200, 2700, 3300, 3900, 4700, 5600, 6800, 8200, (µF) .01, .012, .015, .018, .022, .027, .033, .039, .047, .056, .068, .082

Notes: Other values are available below 10pF. For requirements not shown, please contact your local Murata Erie Sales Office

CONFORMAL COATED RADIAL LEADS
RPE Series

X7R

DIMENSIONS: in. (mm)												
												
MURATA ERIE DESIGNATION	**RPE 110**				**RPE 121/RPE 122**				**RPE 123**			
L	.138 (3.5)				.200 (5.1)				.300 (7.6)			
H	.120 (3.1)				.250 (6.4)				.275 (7.0)			
T	.100 (2.5)				.125 (3.2)				.125 (3.2)			
L.S.	.100 (2.5)				.100 (2.5) / .200 (5.1)				.200 (5.1)			
WVDC	50	100	200	500	50	100	200	500	50	100	200	500
Capacitance	220 – 033	220 – 012	150 – 5600	N/A	220 – 27	220 – 1	220 – 033	220 – 01	15 – 47	056 – 15	8200 – 082	N/A

Capacitance scale: (pF) 100, 120, 150, 180, 220, 270, 330, 390, 470, 560, 680, 820, 1000, 1200, 1500, 1800, 2200, 2700, 3300, 3900, 4700, 5600, 6800, 8200, (μF) .01, 012, 015, 018, 022, 027, 033, 039, 047, 056, 068, 082, .1, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82, 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2

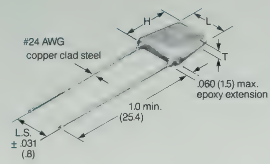
Note: For requirements not shown, please contact your local Murata Erie Sales Office.

CONFORMAL COATED RADIAL LEADS
RPE Series

muRata ERIE

X7R

DIMENSIONS:
in. (mm)



Standard package and lead configurations shown. Other variations and tape and reel data are displayed on pages 44-45. All RPE wire is tinned copper clad steel wire. For other requirements, please contact your local sales office.

MURATA ERIE DESIGNATION	RPE 113				RPE 114				RPE 117			
L	.300 (7.6)				.400 (10.2)				.500 (12.7)			
H	.300 (7.6)				.400 (10.2)				.500 (12.7)			
T	.157 (4.0)				.157 (4.0)				.200 (5.1)			
L.S.	.200 (5.1)				.200 (5.1)				.400 (10.2)			
WVDC	50	100	200	500	50	100	200	500	50	100	200	500
Capacitance	.039 – 1.0	.039 – .47	.018 – .18	4700 – .033	.33 – 2.2	.39 – 1.0	.22 – .56	.022 – 1	1.0 – 2.2	68 – 2.2	.22 – 1.2	.068 – 22

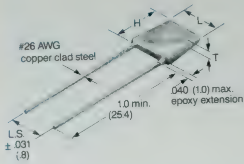
Note: For requirements not shown, please contact your local Murata Erie Sales Office.

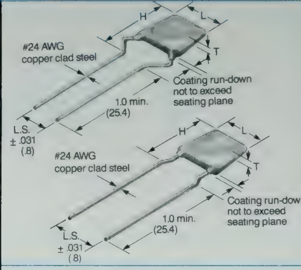
CONFORMAL COATED RADIAL LEADS

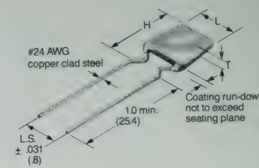
RPE Series

Z5U

DIMENSIONS:
in. (mm)







MURATA ERIE DESIGNATION	RPE 110				RPE 121/RPE 122				RPE 123			
L	.138 (3.5)				.200 (5.1)				.300 (7.6)			
H	.120 (3.1)				.250 (6.4)				.275 (7.0)			
T	.100 (2.5)				.125 (3.2)				.125 (3.2)			
L.S.	.100 (2.5)				.100 (2.5) / .200 (5.1)				.200 (5.1)			
WVDC	50	100	200	500	50	100	200	500	50	100	200	500
Capacitance (from)	1000	1000	1000	N/A	1000	1000	1000	1000	.39	068	.018	N/A
Capacitance (to)	068	015	5600		39	1	033	5600	1.0	15	.033	

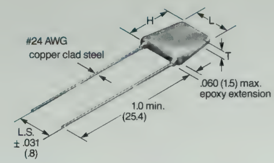
Capacitance scale:
(pF) 1000, 1200, 1500, 1800, 2200, 2700, 3300, 3900, 4700, 5600, 6800, 8200
(μF) .01, .012, .015, .018, .022, .027, .033, .039, .047, .056, .068, .082
.1, .12, .15, .18, 22, .27, .33, 39, .47, .56, .68, 82
1.0, 1.2, 1.5, 1 8, 2 2, 2 7, 3 3, 3 9, 4 7, 5.6, 6 8, 8.2
10.0, 12 0, 15 0, 18 0, 22 0, 27 0, 33.0, 39.0, 47 0, 56 0, 68 0, 82 0

Note: For requirements not shown, please contact your local Murata Erie Sales Office.

RPE Series

Z5U

DIMENSIONS:
in. (mm)



Standard package and lead configurations shown. Other variations and tape and reel data are displayed on pages 44-45. All RPE wire is tinned copper clad steel wire. For other requirements, please contact your local sales office.

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H	.300 (7.6)				.400 (10.2)				.500 (12.7)			
T	.157 (4.0)				.157 (4.0)				.200 (5.1)			
L.S.	.200 (5.1)				.200 (5.1)				.400 (10.2)			
WVDC	50	100	200	500	50	100	200	500	50	100	200	500
Capacitance	.22 – 1.5	.1 – .68	.047 – .15	5600 – .033	82 – 3.3	33 – 1.2	.18 – .56	22 – .1	4.7 – 5.6	1.5 – 2.2	22 – 1.0	12 – 22

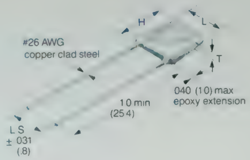
Capacitance scale: (pF) 1000, 1200, 1500, 1800, 2200, 2700, 3300, 3900, 4700, 5600, 6800, 8200; (µF) .01, .012, .015, .018, .022, .027, .033, .039, .047, .056, .068, .082, .1, .12, .15, .18, .22, .27, .33, .39, .47, .56, .68, .82, 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2, 10.0, 12.0, 15.0, 18.0, 22.0, 27.0, 33.0, 39.0, 47.0, 56.0, 68.0, 82.0

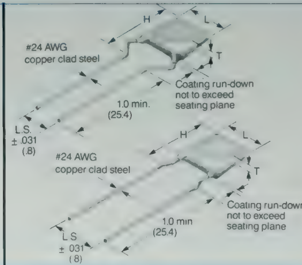
Note: For requirements not shown, please contact your local Murata Erie Sales Office.

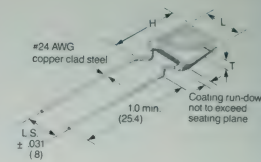
RPE Series

Y5V

DIMENSIONS:
in. (mm)



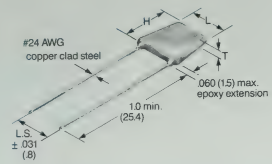




MURATA ERIE DESIGNATION	RPE 110		RPE 121/RPE 122		RPE 123	
L	.138 (3.5)		.200 (5.1)		.300 (7.6)	
H	.120 (3.1)		.250 (6.4)		.275 (7.0)	
T	.100 (2.5)		.125 (3.2)		.125 (3.2)	
L.S.	.100 (2.5)		.100 (2.5) / .200 (5.1)		.200 (5.1)	
WVDC	50	100	50	100	50	100

Note: For requirements not shown, please contact your local Murata Erie Sales Office.

DIMENSIONS:
in. (mm)



Standard package and lead configurations shown. Other variations and tape and reel data are displayed on pages 44-45. All RPE wire is tinned copper clad steel wire. For other requirements, please contact your local sales office.

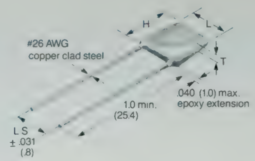
MURATA ERIE DESIGNATION	RPE 113		RPE 114		RPE 117	
L	.300 (7.6)		.400 (10.2)		.500 (12.7)	
H	.300 (7.6)		.400 (10.2)		.500 (12.7)	
T	.157 (4.0)		.157 (4.0)		.200 (5.1)	
L.S.	.200 (5.1)		.200 (5.1)		.400 (10.2)	
WVDC	50	100	50	100	50	100

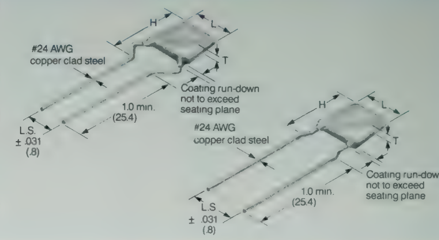
Note: For requirements not shown, please contact your local Murata Erie Sales Office.

CONFORMAL COATED RADIAL LEADS
RPE Series

TEMPERATURE COMPENSATING

DIMENSIONS: in. (mm)

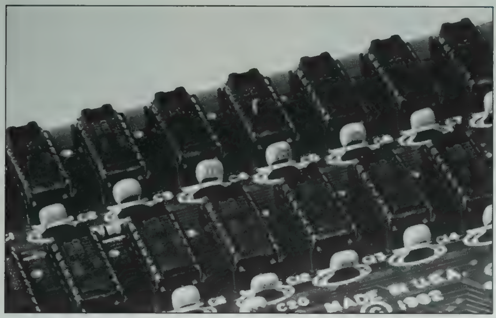




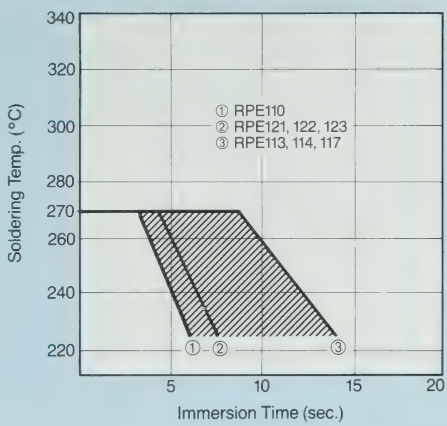
MURATA ERIE DESIGNATION	RPE 110		RPE 121/RPE 122	
L	.138 (3.5)		.200 (5.1)	
H	.120 (3.1)		.250 (6.4)	
T	.100 (2.5)		.125 (3.2)	
L.S.	.100 (2.5)		.100 (2.5) / .200 (5.1)	
WVDC	50	100	50	100
TC: N150 (P2H) Cap. Range: (pF)	1 – 360	1 – 360	1 – 2400	1 – 2200
TC: N220 (R2H) Cap. Range: (pF)	1 – 560	1 – 510	1 – 2700	1 – 2400
TC: N330 (S2H) Cap. Range: (pF)	1 – 470	1 – 430	1 – 3300	1 – 3000
TC: N470 (T2H) Cap. Range: (pF)	1 – 390	1 – 510	1200	240
TC: N750 (U2J) Cap. Range: (pF)	1 – 1800	1 – 960	15 – 7500	15 – 4700

APPLICATION NOTES

RADIAL LEAD
RPE Series



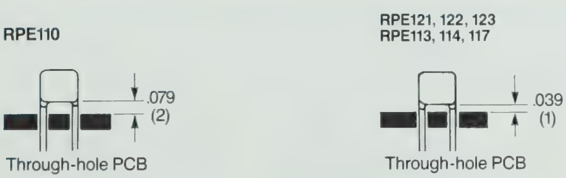
1. Allowable Conditions for Soldering Temperature vs. Time
   Perform soldering within tolerance range (shaded area).



2. A) Do not impose a tensile load on the lead wire during solder heat exposure.

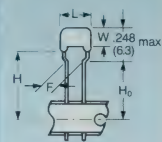
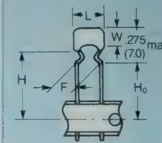
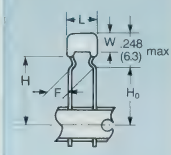
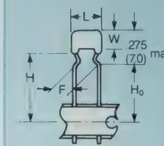
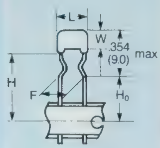
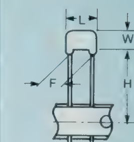
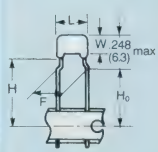
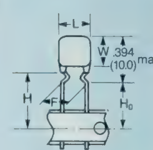
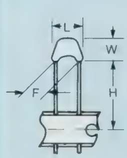
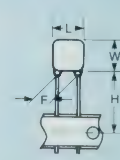
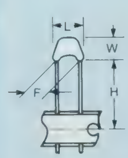
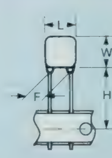
   B) For RPE110, set base of lead .079 (2) and for RPE121/122, set base of lead .040 (1.0) above printed circuit board surface per diagram:

DIMENSIONS: in. (mm)

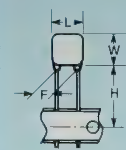
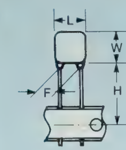
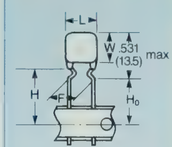
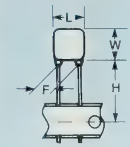


CONFORMAL COATED RADIAL LEADS

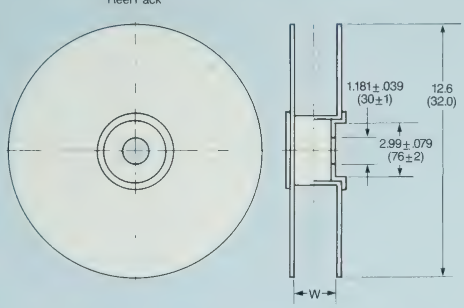
TAPE & REEL for AUTO INSERTION

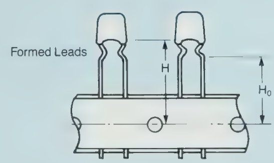
DIMENSIONS: in. (mm)	Style/Variation Outline	DIMENSIONS: in. (mm)	Style/Variation Outline
RPE 121-911 L: .197 (5.0) max. W: .197 (5.0) max. T: .124 (3.15) max. F: .098 (2.5) + .016 (0.4) − .008 (0.2) H_0: .630 (16.0) ± .020 (0.5) H: .709 (18.0) ± .039 (1.0)		**RPE 123-901** L: .295 (7.5) max. W: .216 (5.5) max. T: .124 (3.15) max. F: .205 (5.2) ± .016 (0.4) H_0: .630 (16.0) ± .020 (0.5) H: .709 (18.0) ± .039 (1.0)	
RPE 122-901 L: .197 (5.0) max. W: .197 (5.0) max. T: .124 (3.15) max. F: .205 (5.2) ± .016 (0.4) H_0: .630 (16.0) ± .020 (0.5) H: .709 (18.0) ± .039 (1.0)		**RPE 123-906** L: .295 (7.5) max. W: .216 (5.5) max. T: .124 (3.15) max. F: .205 (5.2) ± .016 (0.4) H_0: .787 (20.0) ± .020 (0.5) H: .866 (22.0) ± .039 (1.0)	
RPE 122-905 L: .197 (5.0) max. W: .197 (5.0) max. T: .124 (3.15) max. F: .205 (5.2) ± .016 (0.4) H_0: .630 (16.0) ± .020 (0.5) H: .787 (20.0) ± .039 (1.0)		**RPE 123-977** L: .295 (7.5) max. W: .216 (5.5) max. T: .124 (3.15) max. F: .205 (5.2) ± .016 (0.4) H: .787 (20.0) ± .020 (0.5)	
RPE 122-906 L: .197 (5.0) max. W: .197 (5.0) max. T: .124 (3.15) max. F: .205 (5.2) ± .016 (0.4) H_0: .787 (20.0) ± .020 (0.5) H: .866 (22.0) ± .039 (1.0)		**RPE 113-901** L: .295 (7.5) max. W: .295 (7.5) max. T: .157 (4.0) max. F: .205 (5.2) ± .016 (0.4) H_0: .630 (16.0) ± .020 (0.5) H: .748 (19.0) ± .039 (1.0)	
RPE 122-977 L: .197 (5.0) max. W: .197 (5.0) max. T: .124 (3.15) max. F: .205 (5.2) ± .016 (0.4) H: .787 (20.0) ± .020 (0.5)		**RPE 113-902** L: .295 (7.5) max. W: .295 (7.5) max. T: .157 (4.0) max. F: .205 (5.2) ± .016 (0.4) H: .650 (16.5) ± .020 (0.5)	
RPE 122-978 L: .197 (5.0) max. W: .197 (5.0) max. T: .124 (3.15) max. F: .205 (5.2) ± .016 (0.4) H: .650 (16.5) ± .020 (0.5)		**RPE 113-903** L: .295 (7.5) max. W: .295 (7.5) max. T: .157 (4.0) max. F: .205 (5.2) ± .016 (0.4) H: .689 (17.5) ± .020 (0.5)	

CONFORMAL COATED RADIAL LEADS
TAPE & REEL for AUTO INSERTION

DIMENSIONS: in. (mm)	Style/Variation Outline	DIMENSIONS: in. (mm)	Style/Variation Outline
RPE 113-907 L: .295 (7.5) max. W: .295 (7.5) max. T: .157 (4.0) max. F: .205 (5.2) ± .016 (0.4) H: .787 (20.0) ± .020 (0.5)		**RPE 114-903** L: .40 (10.2) max. W: .40 (10.2) max. T: .157 (4.0) max. F: .205 (5.2) ± .016 (0.4) H: .689 (17.5) ± .020 (0.5)	
RPE 114-901 L: .40 (10.2) max. W: .40 (10.2) max. T: .157 (4.0) max. F: .205 (5.2) ± .016 (0.4) H_0: .630 (16.0) ± .020 (0.5) H: .748 (19.0) ± .039 (1.0)		**RPE 114-907** L: .394 (10.0) max. W: .394 (10.0) max. T: .157 (4.0) max. F: .205 (5.2) ± .016 (0.4) H: .787 (20.0) ± .020 (0.5)	

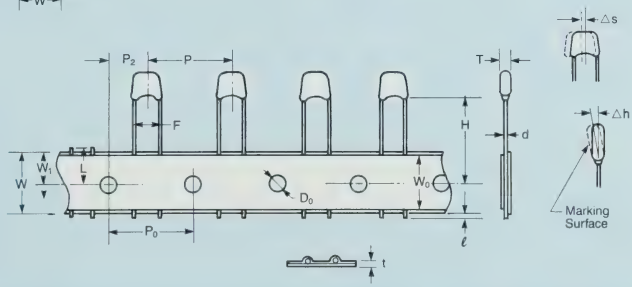
TAPE & REEL DIMENSIONS: in. (mm)





STANDARD QUANTITY PER REEL

Type & Size	Reel	Ammo
RPE 121	2500	2000
RPE 122	2500	2000
RPE 123	2500	2000
RPE 113	2000	2000
RPE 114	1500	1500



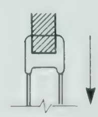
Taping Pitch P	Feed Hole Pitch P_0	Feed Hole Position P_2	Deviation Along Tape $\triangle S$	Width of Tape Carrier W	Half Width of Tape Carrier W_1	Lead Protrusion ℓ	Diameter of Feed Hole D_0	Total Tape Thickness t	Deviation Across Tape $\triangle h$	Cutting Position Failure L	Width of Masking Tape W_0	Margin Between Tape W_2
.500	.500 ±.008	.250 ±.051	±.079	.709 ±.020	$.354^{+0}_{-.020}$	−.039 to .020 (−1.0 to 0.5)	.157±.004 (4.0±0.1)	.028±.008 (0.7±0.2)	±.039 (±1.0)	$.433^{+0}_{-.039}$ ($11.0^{+0}_{-1.0}$)	.492 (12.5 min.)	.059±.059 (1.5±1.5)

SPECIFICATIONS

GENERAL

TEST	SPECIFICATIONS	T.C. Tolerance Capacitance (pF)*	T.C. Tolerance (ppm)
Operating Temperature Range	COG: –55°C to +125°C P2H: –55°C to +85°C R2H: –55°C to +85°C S2H: –55°C to +85°C T2H: –55°C to +85°C U2J: –55°C to +85°C X7R: –55°C to +125°C Z5U: +10°C to +85°C Y5V: –30°C to +85°C		
Temperature Coefficient	COG: 0±30ppm/°C over temp. range of –55°C to +125°C P2H: N150±60ppm/°C over temp. range of –55°C to +85°C R2H: N220±60ppm/°C over temp. range of –55°C to +85°C S2H: N330±60ppm/°C over temp. range of –55°C to +85°C T2H: N470±60ppm/°C over temp. range of –55°C to +85°C U2J: N750±120ppm/°C over temp. range of –55°C to +85°C	10 and over 4.0-9.9 2.1-3.9 .4-2.0	± 30(G) ± 60(H) ±120(J) ±250(K)
	X7R: ±15% over temp. range of –55°C to +125°C Z5U: +22, –56% over temp. range of –10°C to +85°C Y5V: +22, –82% over temp. range of –30°C to +85°C	*Refer to EIA RS198 for limitations.	

MECHANICAL

TEST	TEST METHOD	REQUIREMENT
Lead Pull Strength	MIL-STD-202, Method 211A, Test Condition A	Radial direction: RPE 110: 2 lb. min. others: 5 lb. min. 
Solderability	MIL-STD-202, Method 208F.	Lead wire will exhibit >95% coverage on conformal coated units.
Resistance to Soldering Heat	MIL-STD-202, 210A Parts are immersed in solder bath: RPE 110, 270±5°C for 3±0.5 sec. All other RPE types: 350±10°C for 3±0.5 sec.	Appearance: No Damage ΔC: COG=±0.25pF or ±2.5% (whichever is greater). X7R=±7.5% max. Z5U ±20% max. Y5V=±20% max. After 48±4 hour period, parts should satisfy all initial requirements for D.F., I.R., and Flash Voltage (2.5xWV). (500V=2xWV). 25% max. leaching on each edge.
Vibration	MIL-STD-202 method 204D condition B 10-2,000 Hz, 15 G's	Appearance: No Damage Initial value guarantee
Shock	MIL-STD-202 Method 213B, Condition I	Appearance: No Damage Initial value guarantee

ELECTRICAL

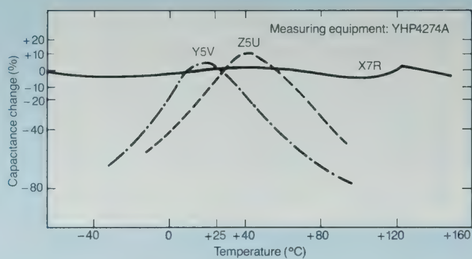
TEST	TEST METHOD	REQUIREMENT
Capacitance (Voltage and Frequency)	COG: over 1,000pF 1KHz±100Hz, 1±0.2Vrms up to 1,000pF 1MHz±100KHz, 1±0.2Vrms X7R: 1KHz±100Hz, 1±0.2Vrms Z5U/Y5V: 1KHz±100Hz, .5V±.1Vrms	
Q/Dissipation Factor (Volt. & Freq. same as Cap. Test)	COG: (less than 30pF), Q≥400+(20•C(pF)) @ 25°C (30pF and over), Q ≥1,000 @ 25°C X7R: D.F.=2.5% max. @ 25°C Z5U: D.F.=3.0% max. @ 25°C, (5.0% max. @ 25°C for RPE200 Series) Y5V: D.F.=3.5% max. @ 25°C	
Insulation Resistance	Apply rated voltage for max. of 2 min. with 50mA limiting current.	COG, X7R: 100,000MΩ or 1,000MΩ•μF (whichever is less). Z5U, Y5V: 10,000MΩ or 500MΩ•μF (whichever is less).
Dielectric Strength	2.5xWV for 5 sec. with a series resistor limiting the charging current to 50mA max. (500V=WVx2)	No dielectric breakdown
Typical Aging Rate (ΔC per decade hour)	COG: negligible X7R: –3.0% Z5U: –5.0% Y5V: –7.0%	

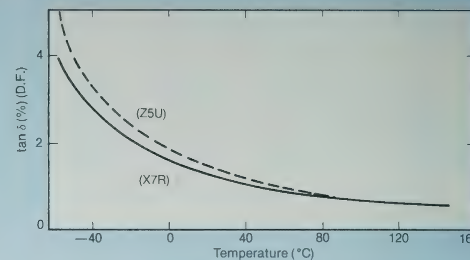
ENVIRONMENTAL

TEST	TEST METHOD	REQUIREMENT
Thermal Shock	MIL-STD-202, method 107, condition A Prior to starting Thermal Shock test, capacitors shall be heat treated (deaged) for one (1) hour at 150°C. Allow capacitors to stabilize at room temperature for 24 hours prior to taking initial measurements. Post thermal Shock measurement shall be taken after 24 hours stabilization.	Appearance: No visual damage ΔC: COG=±2.0% or ±0.5pF (whichever is greater) X7R=±12.5% Z5U=±20.0% Y5V=±30.0% Q: COG=1,000 min. (>30pF) 400+(20•C(pF)) (≤30pF) D.F.: X7R=2.5% max. @ 25°C, Z5U=3.0% max. @ 25°C, (5.0% max. @ 25°C for RPE200 Series) Y5V=5.0% max. @ 25°C I.R.: COG/X7R=100,000MΩ min. or 1,000MΩ•μF (whichever is less) Z5U/Y5V=10,000MΩ or 500Ω•μF min. (whichever is less)
Humidity (No Load) **Humidity (Load)** **Life Test**	500±12 hours at 40±2°C in 90 to 95% humidity. 500±12 hours at 40±2°C in 90 to 95% humidity with rated voltage applied (max. current 50mA) 1,000±12 hours at max. rated temperature with 200% rated voltage applied. Prior to starting Life Test, capacitors shall be voltage treated for 1 hour with 200% rated voltage applied at max. rated temperature. Allow capacitors to stabilize for 24 hours prior to taking initial measurements. Post Life Test measurements shall be taken after 24 hours stabilization.	Appearance: No visual damage ΔC: COG=±2.0% or ±0.5pF (whichever is greater) X7R=±12.5% Z5U=±30.0% Y5V=±30.0% Q: COG=500 min. (>30pF) 200+(10•C(pF)) (≤30pF) D.F.: X7R=3.0% max. @ 25°C, Z5U=3.5% max. @ 25°C, (7.5% max. @ 25°C for RPE200 Series) Y5V=7.0% max. @ 25°C, I.R.: COG/X7R=10,000MΩ min. or 100MΩ•μF (whichever is less) Z5U/Y5V=1,000MΩ min. or 500MΩ•μF min. (whichever is less)

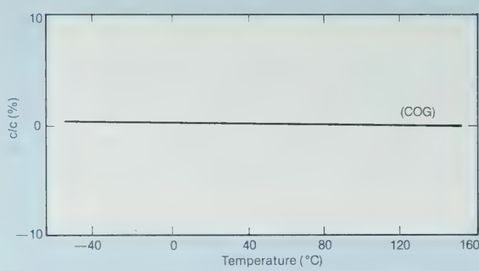
TYPICAL PERFORMANCE CHARACTERISTICS

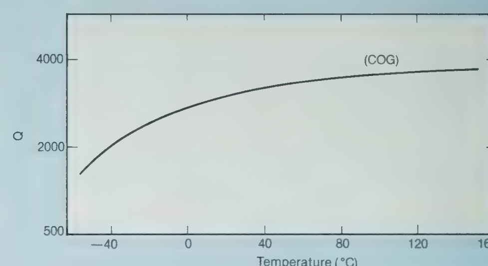
TEMPERATURE VS. CAPACITANCE AND DISSIPATION FACTOR: X7R, Z5U



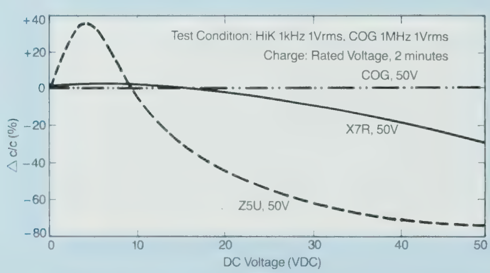


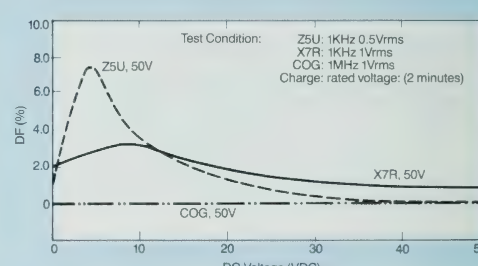
TEMPERATURE VS. CAPACITANCE AND Q:COG (NPO)



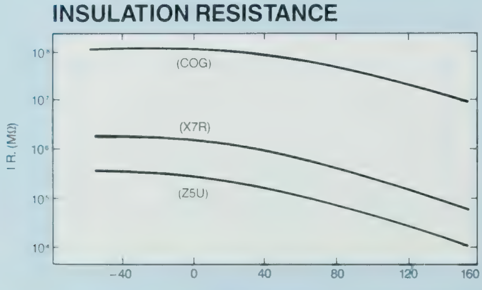


DC VOLTAGE VS. CAPACITANCE AND DISSIPATION FACTOR

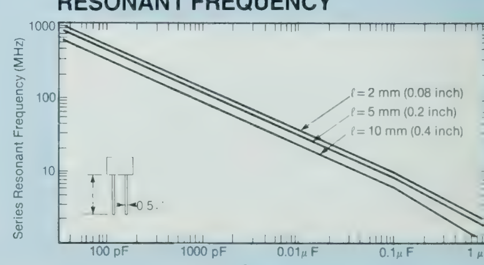




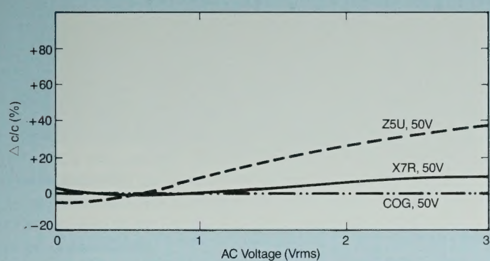
TEMPERATURE VS. INSULATION RESISTANCE

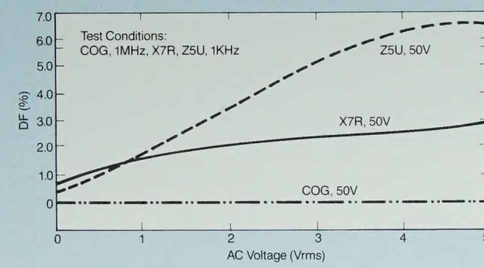


CAPACITANCE VS. SERIES RESONANT FREQUENCY

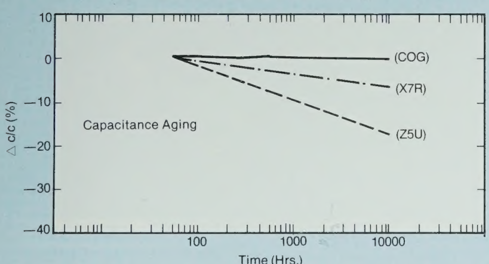


AC VOLTAGE VS. CAPACITANCE AND DISSIPATION FACTOR

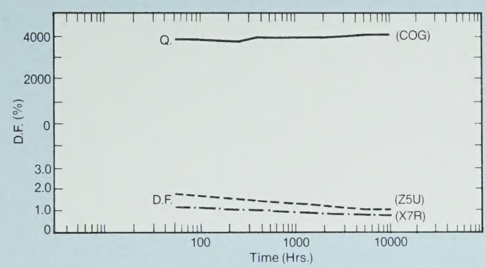




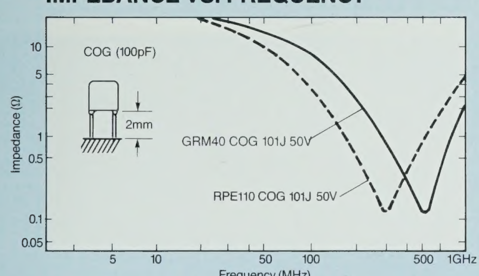
CAPACITANCE VS. TIME (Aging)



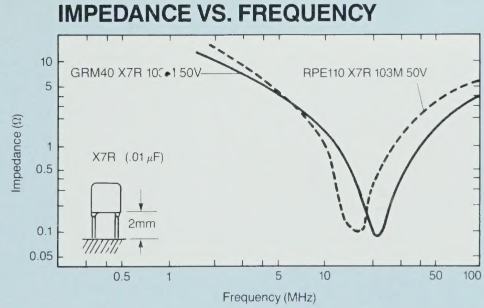
DISSIPATION FACTOR AND Q VS. TIME (Aging)



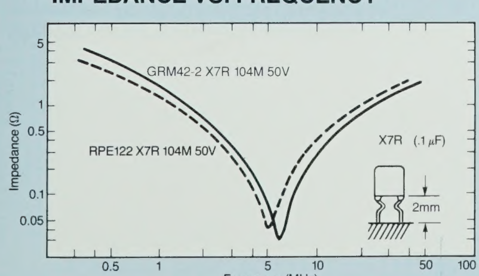
IMPEDANCE VS. FREQUENCY



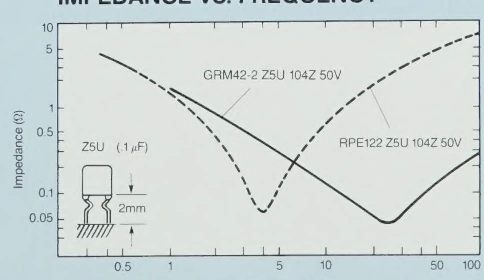
IMPEDANCE VS. FREQUENCY



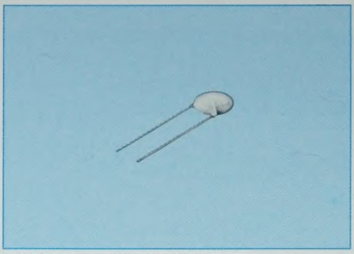
IMPEDANCE VS. FREQUENCY



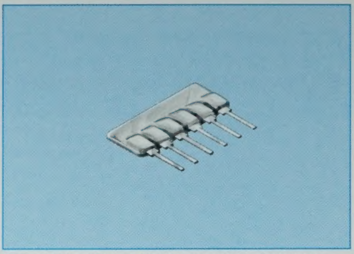
IMPEDANCE VS. FREQUENCY



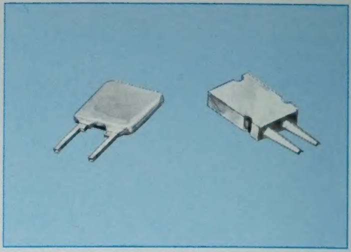
OTHER MURATA ERIE PRODUCTS



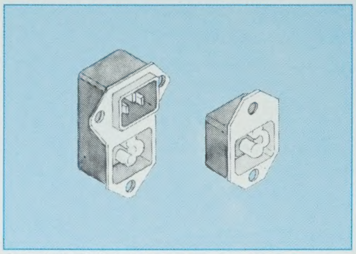
DISC SAFETY CAPACITORS...
Ceramic disc capacitors for bypass and across-line applications. Meet UL, CSA, VDE, etc. specifications.



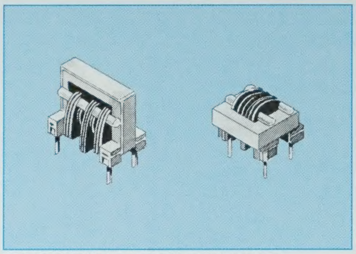
CAPACITORS/RESISTOR NETWORKS...
Single in-line packages in both standard and custom configurations to meet a variety of filtering requirements.



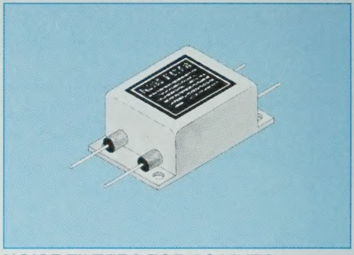
CERAMIC RESONATORS...
for low cost microprocessor applications in low KHz to medium MHz frequency ranges.



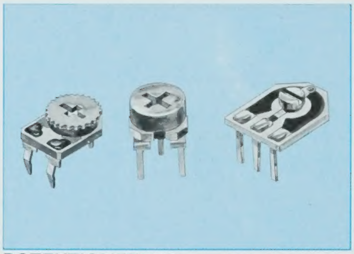
AC LINE FILTERS...
One of industry's broadest lines. Two and three wire units in a large selection of current ratings. UL, CSA and TUV listed.



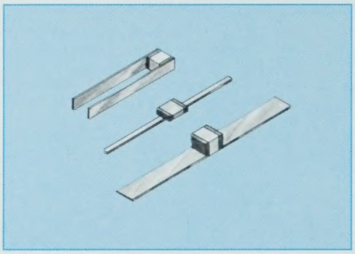
COMMON MODE CHOKE COILS...
A complete selection of common mode choke coils for noise reduction in a wide variety of consumer electronic and data processing equipment.



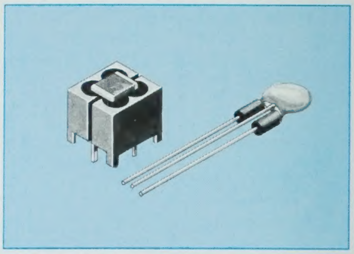
NOISE FILTERS FOR AC LINES...
Complete line of filters to suppress noise from AC lines. Aid in meeting FCC and VDE specifications. Recognized by major safety organizations.



POTENTIOMETERS...
Low cost single-turn trimming potentiometers in many sizes and configurations. Single and multi-turn sealed precision units.



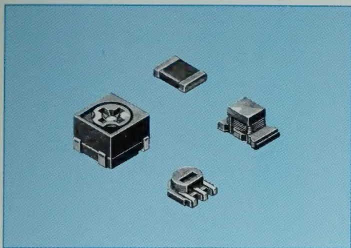
HI-Q CHIPS...
High performance precision components for miniature state-of-the-art microwave circuit applications.



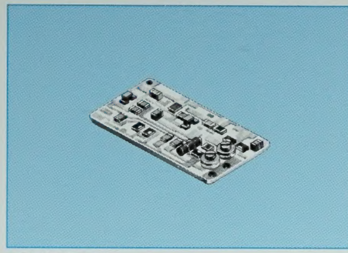
P.C.B. FILTERS...
for EMI/RFI filtering in industrial and commercial applications. Large variety of devices cover the frequency spectrum from power line to 10GHz.

OTHER MURATA ERIE PRODUCTS

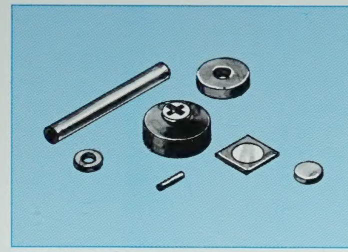
muRata ERIE



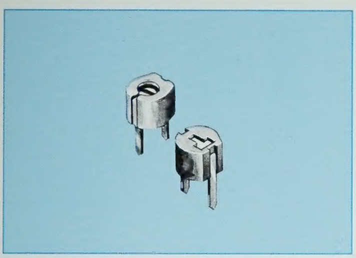
SURFACE MOUNTED COMPONENTS...
Capacitors, inductors, resistors, potentiometers and more for state-of-the-art circuit applications.



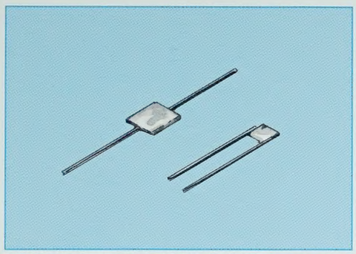
HYBRID I.C.'s...
Custom designed to meet specific application requirements for amplifiers, tuners, control circuits, etc.



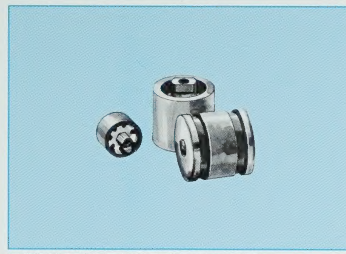
RESOMICS®...
Ceramic microwave dielectric resonators for filters, oscillators, and waveguides to 50GHz with Q's over 10,000.



TZ TRIMCAPS ...
With unique axleless construction provides exceptionally linear T.C.

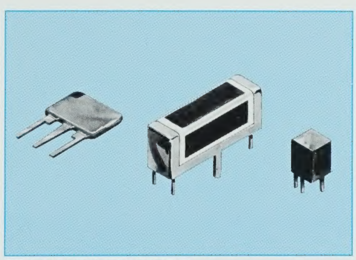


UY UNICERAM MINIATURE CERAMIC CAPACITORS...
Offer the highest available Q for applications where low inductance is essential.

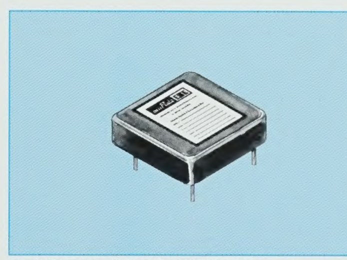


HIGH VOLTAGE CERAMIC CAPACITORS...
From 7.5KV to 40KV in capacities and power handling capabilities for every application requirement.

PIEZO-ALARMS...
For audio signaling applications can be supplied as either cased or uncased units and in a variety of sizes and frequencies.



CERAMIC FILTERS...
For both communications and consumer AM, FM and TV applications in IF and discriminator circuits.



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